

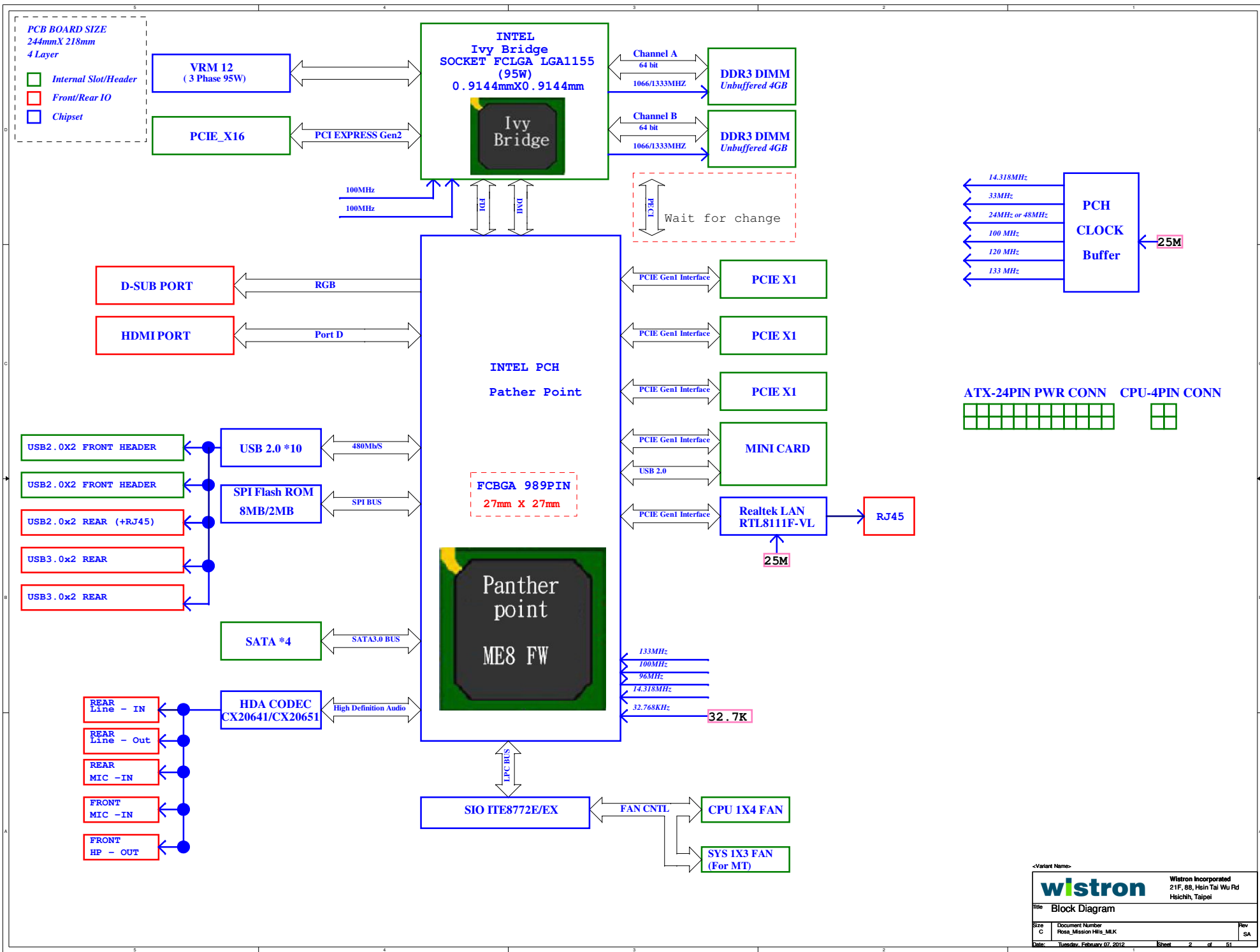
Model: Mission Hills MLK
 PCB Ver: A00
 PCB Number: 11068-1
 PCB P/N:48.3EQ06.011
 SCH Ver:-1
 PCBA:

PAGE	TITLE	Quantity
01	Cover Page	
02	BLOCK DIAGRAM	
03	Power Delivery	
04	POWER GOOD AND RESET DIAGRAM	
05	CLOCKS DIAGRAM	
06	Power Sequence	
07	POWER Map	
08	GPIO	
09	CLOCK GEN - CK505	
10	CPU LGA 1155_1	
11	CPU LGA 1155_2	
12	CPU LGA 1155_3	
13	CPU LGA 1155_4	
14	XDP/80 PORT HEADER	
15	DDR3 CHA DIMM 0	
16	TBD	
17	DDR3 CHB DIMM 0	
18	TBD	
19	PCH Pather AUDIO/GPIO/SPI	
20	PCH Pather_CLK/FDI/ONFI/USB3	
21	PCH Pather SATA/FAN/DP	
22	PCH Pather PCI/PCIE/DMI/USB	
23	PCH Pather GND/STRAPS	
24	PCH Pather POWER	
25	SATA Port	
26	PCIEX16 CONNECTOR	
27	VGA Port	
28	HDMI Port	
29	TBD	
30	FRONT USB	
31	USB+RJ45	
32	Gb LAN RTL8111F	
33	AUDIO CX20641/CX20651	
34	AUDIO CODEC JACKS	
35	DSW	
36	SIO ITE8772	
37	TBD	
38	TBD	
39	FAN CIRCUITS/HOLE	
40	TBD	
41	PCIEX1 CONNECTOR	
42	Mini PCIE Slot	
43	REAR USB30_1	
44	REAR USB30_2	
45	PWR/FNT PNL	
46	DUAL POWER	
47	DDR POWER	
48	SYSTEM POWER	
49	CPU VTT & CPU SA	
50	CPU VRD 12-1 & CPU_AXG	
51	CPU_VRD 12-2	

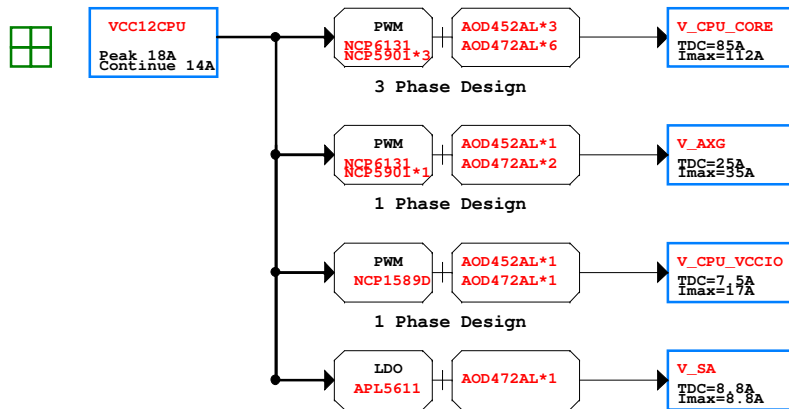
PCB BOARD SIZE
 4 Layers
 244mmX 218mm

BOM Configuration
 Unmount: (R)
 Unmount after MP (X)

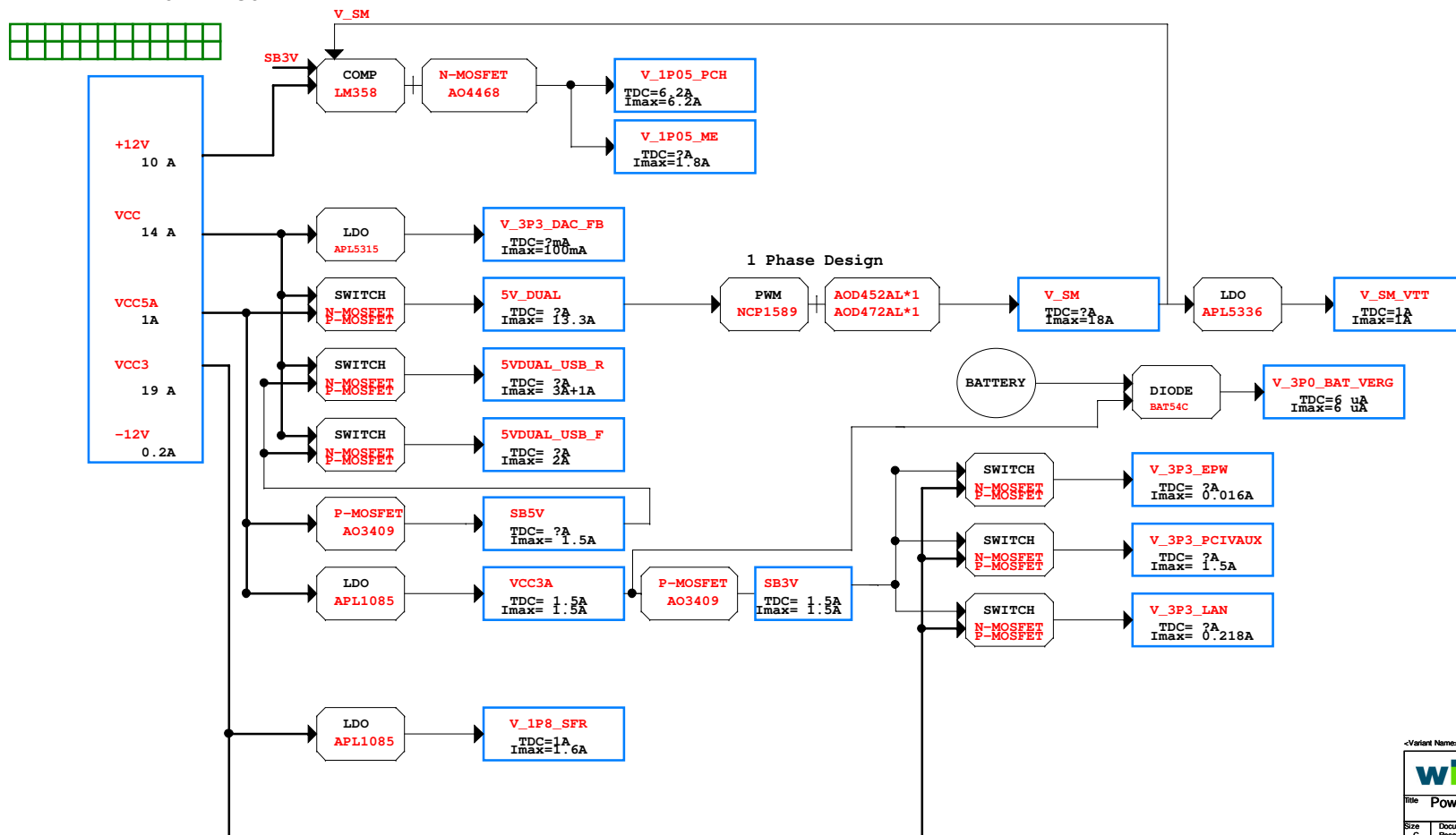
SA BUILD
 Maho Bay :
 LGA1155 : Ivy Brighe
 Chipset :Pather Point B75
 LAN : Gb LAN RTL8111F



CPU 2X2 POWER CONN



ATX 2X12 POWER CONN



<Variant Name>

wistron

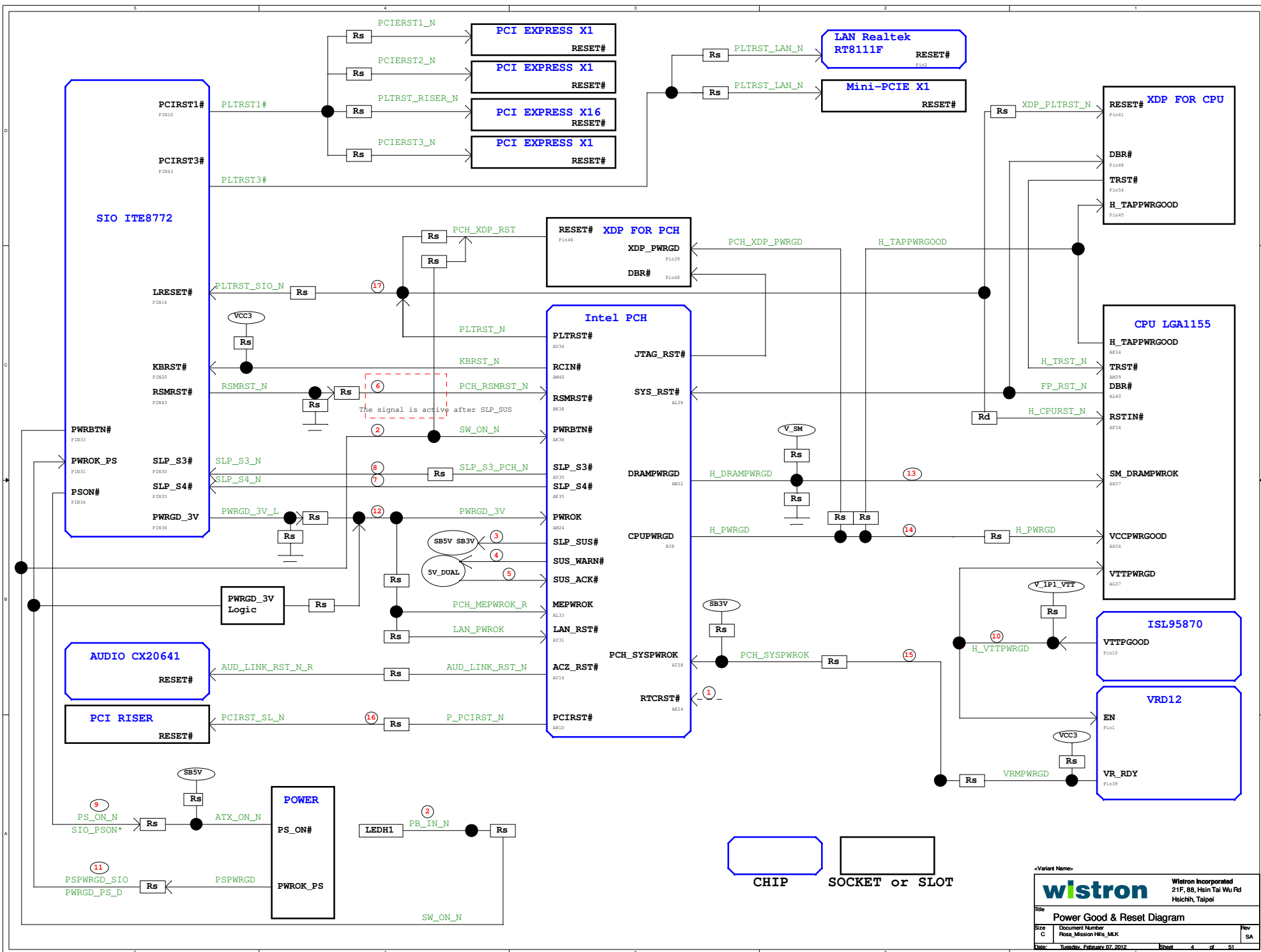
Wistron Incorporated
21F, 88, Hei Tai Wu Rd
Hsichih, Taipei

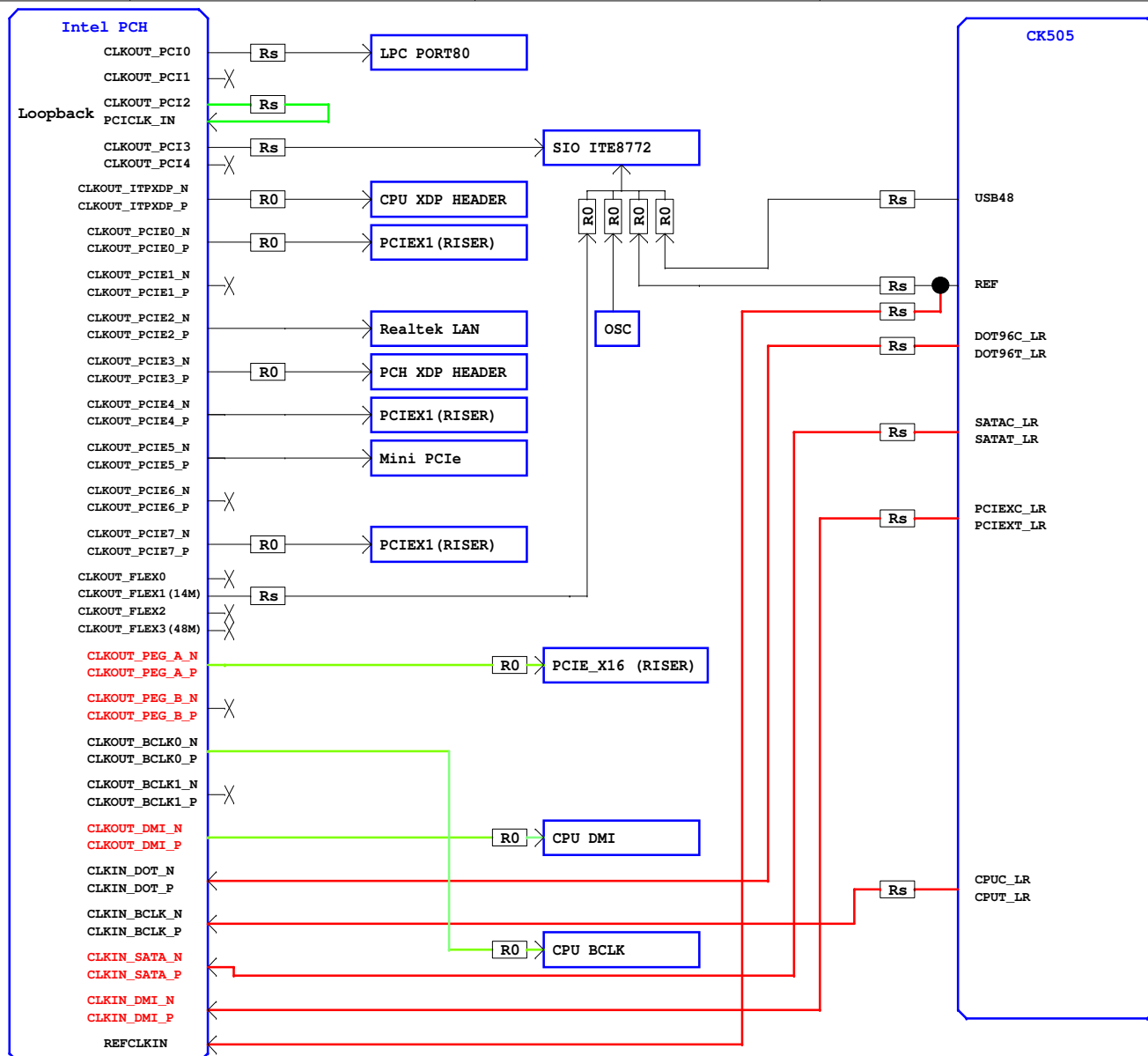
Title Power Delivery

Size C Document Number
Pesa_Mission_Hills_MLK

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SA

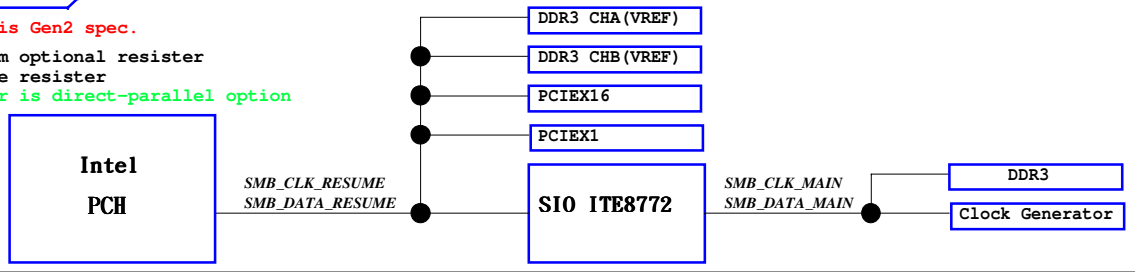
Date: Tuesday, February 07, 2012 Sheet 3 of 51



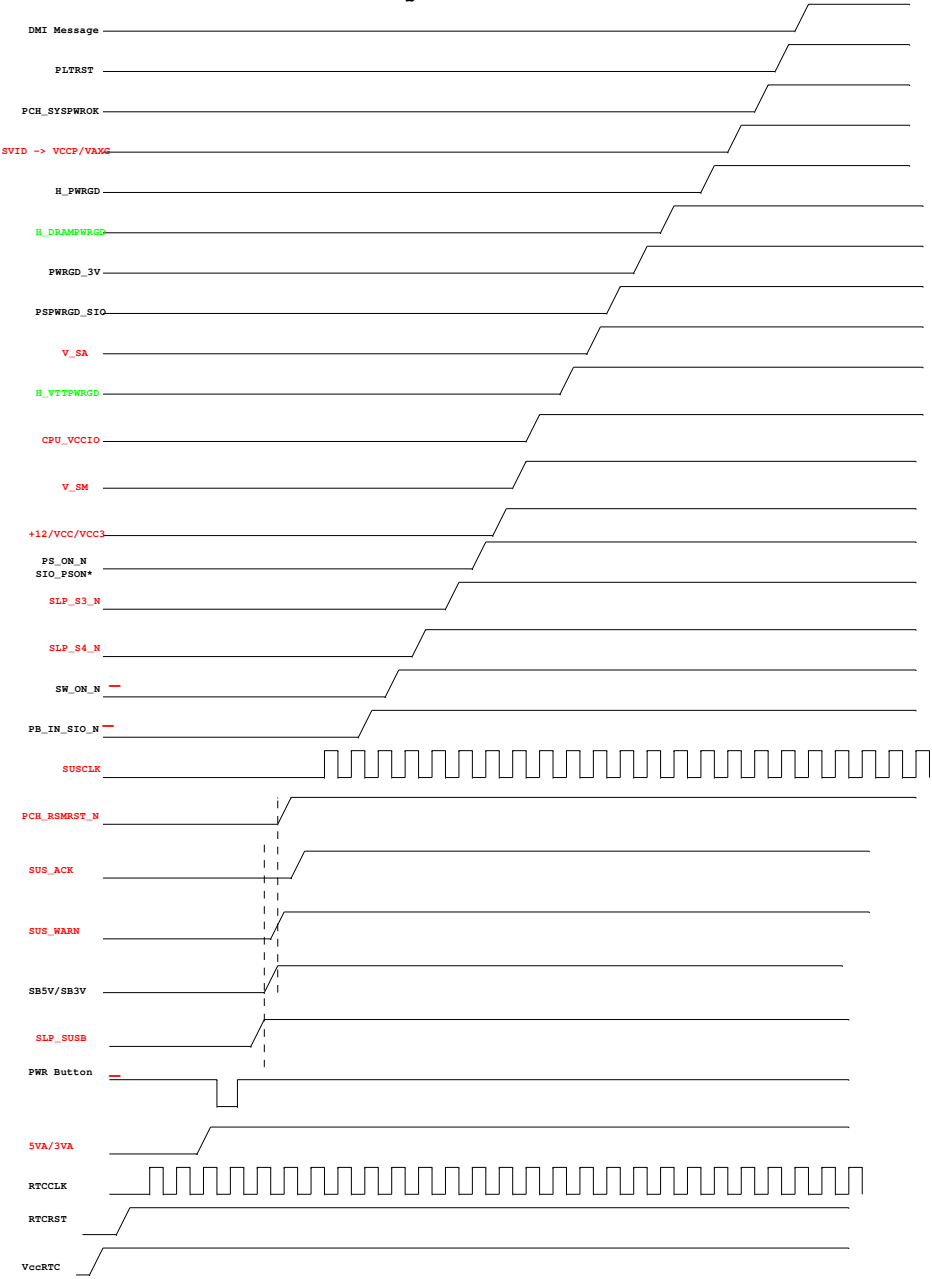


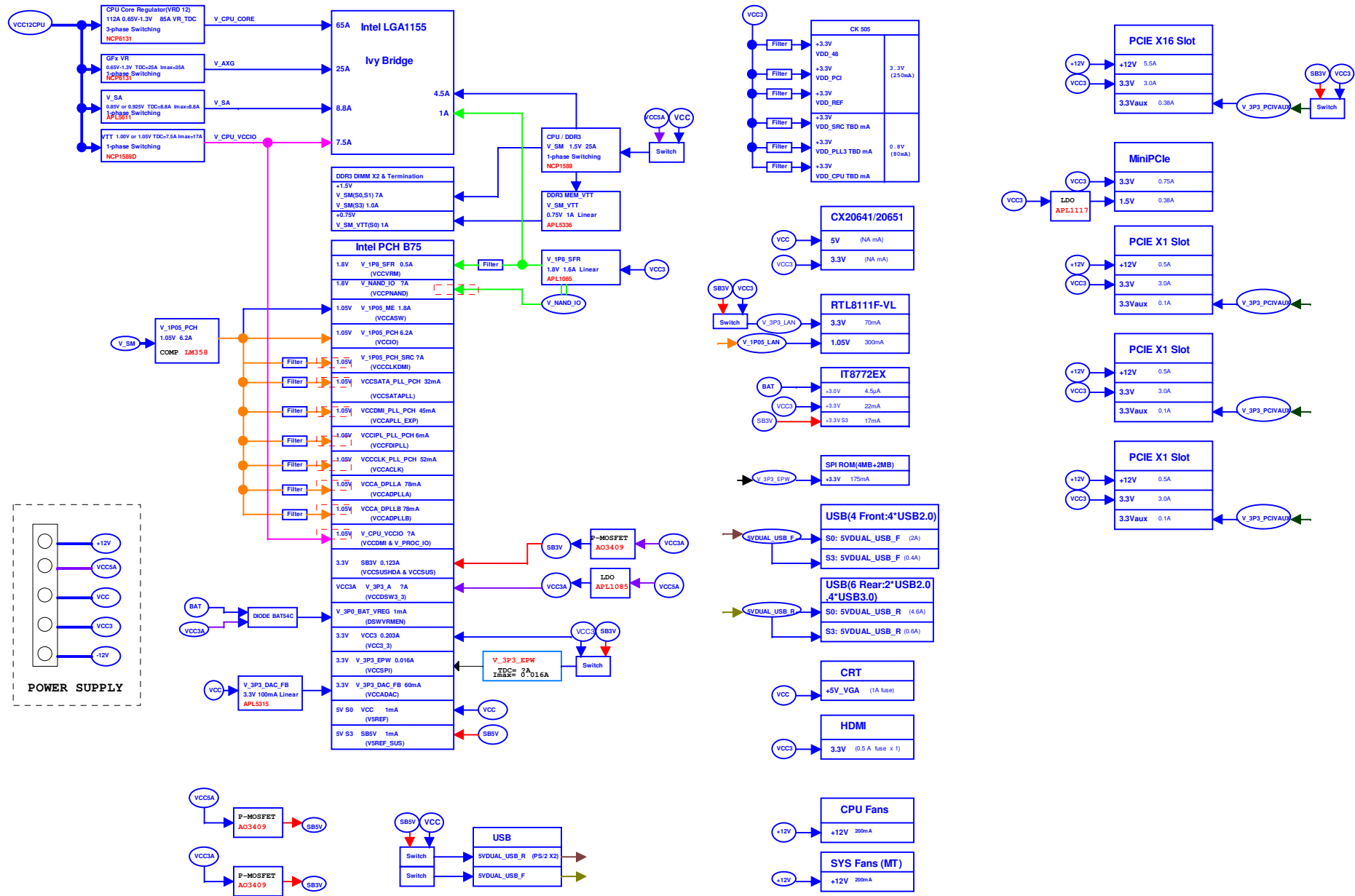
BTM: Buffer Through Mode
 Need CK505 to provide 4 clock to PCH
 FCIM: Full Clock Intergration Mode
 Remove CK505

Note: Red Color is Gen2 spec.
 Note: R0 is 0 ohm optional resistor
 Note: Rs is serie resistor
 Note: Green Color is direct-parallel option



POWER ON SEQUENCE



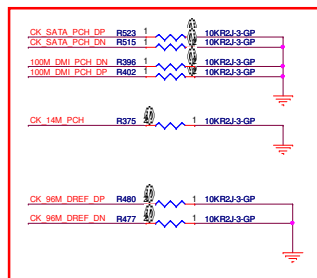


PCH Buffer CLOCK

22 CK_96M_DREF_DP
22 CK_96M_DREF_DN
21 CK_SATA_PCH_DP
21 CK_SATA_PCH_DN
22 100M_DM1_PCH_DP
22 100M_DM1_PCH_DN

14M CLOCK

20 CK_14M_PCH



Terminate PCH CLK Inputs

Remove CLK GEN
Use PCH Internal CLK

<Variant Name>

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Title CLOCK GEN - ICS9LRS4180

Size
C

Document Number
Pesa_Mission Hills_MLK

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DDR DATA

15 M_DATA_A[0..63] <<>
17 M_DATA_B[0..63] <<>
15 M_DQS_A_DP[0..8] <<>
15 M_DQS_A_DN[0..8] <<>
17 M_DQS_B_DP[0..8] <<>
17 M_DQS_B_DN[0..8] <<>

DDR CMD/ADD

15 M_MAA_A[0..15] <<>
17 M_MAA_B[0..15] <<>
15 M_WE_A_N <<>
15 M_CAS_A_N <<>
15 M_RAS_A_N <<>
15 M_SBS_A1 <<>
15 M_SBS_A2 <<>
17 M_WE_B_N <<>
17 M_CAS_B_N <<>
17 M_RAS_B_N <<>
17 M_SBS_B0 <<>
17 M_SBS_B1 <<>
17 M_SBS_B2 <<>

DDR CTRL

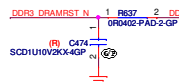
15 M_SCs_A_N0 <<>
15 M_SCs_A_N1 <<>
15 M_SCKE_A0 <<>
15 M_SCKE_A1 <<>
15 M_ODT_A0 <<>
15 M_ODT_A1 <<>
17 M_SCs_B_N0 <<>
17 M_SCs_B_N1 <<>
17 M_SCKE_B0 <<>
17 M_SCKE_B1 <<>
17 M_ODT_B0 <<>
17 M_ODT_B1 <<>

DDR CLOCK

15 CK_M_DDR0_A_DP <<>
15 CK_M_DDR0_A_DN <<>
15 CK_M_DDR1_A_DP <<>
15 CK_M_DDR1_A_DN <<>
17 CK_M_DDR0_B_DP <<>
17 CK_M_DDR0_B_DN <<>
17 CK_M_DDR1_B_DP <<>
17 CK_M_DDR1_B_DN <<>

DDR OTHERS

15,17 DDR3_DRAMRST_N <<>



Can be left as no connects if no support ECC.

U27A

1 OF 11

M_MAA_A0	AV27	SA_MA_0
M_MAA_A1	AV24	SA_MA_1
M_MAA_A2	AW24	SA_MA_2
M_MAA_A3	AW23	SA_MA_3
M_MAA_A4	AV23	SA_MA_4
M_MAA_A5	AT24	SA_MA_5
M_MAA_A6	AT23	SA_MA_6
M_MAA_A7	AV22	SA_MA_7
M_MAA_A8	AV22	SA_MA_8
M_MAA_A9	AT22	SA_MA_9
M_MAA_A10	AV28	SA_MA_10
M_MAA_A11	AT21	SA_MA_11
M_MAA_A12	AT21	SA_MA_12
M_MAA_A13	AW32	SA_MA_13
M_MAA_A14	AV20	SA_MA_14
M_MAA_A15	AT20	SA_MA_15
M_WE_A_N	AW29	SA_WE#
M_CAS_A_N	AV30	SA_CAS#
M_RAS_A_N	AV25	SA_RAS#
M_SBS_A0	AV29	SA_BS_0
M_SBS_A1	AV28	SA_BS_1
M_SBS_A2	AV20	SA_BS_2
M_SCs_A_N0	AV29	SA_CS#_0
M_SCs_A_N1	AV30	SA_CS#_1
M_SCKE_A0	AV29	SA_CS#_2
M_SCKE_A1	AV28	SA_CS#_3
M_SCKE_A0	AV19	SA_CKE_0
M_SCKE_A1	AV18	SA_CKE_1
M_SCKE_A0	AV18	SA_CKE_3
M_ODT_A0	AV31	SA_ODT_0
M_ODT_A1	AV30	SA_ODT_1
M_ODT_A0	AV33	SA_ODT_2
M_ODT_A1	AV33	SA_ODT_3
CK_M_DDR0_A_DP	AV25	SA_CK_0
CK_M_DDR0_A_DN	AV25	SA_CK#_0
CK_M_DDR1_A_DP	AV25	SA_CK_1
CK_M_DDR1_A_DN	AV25	SA_CK#_1
CK_M_DDR0_B_DP	AV27	SA_CK_2
CK_M_DDR0_B_DN	AV26	SA_CK#_2
CK_M_DDR1_B_DP	AV26	SA_CK_3
CK_M_DDR1_B_DN	AV26	SA_CK#_3

SAN 100NF
(62-10055-441)

DDR3

U27B

2 OF 11

M_MAA_B0	AK24	SB_MA_0
M_MAA_B1	AK20	SB_MA_1
M_MAA_B2	AM19	SB_MA_2
M_MAA_B3	AK18	SB_MA_3
M_MAA_B4	AP19	SB_MA_4
M_MAA_B5	AP18	SB_MA_5
M_MAA_B6	AM18	SB_MA_6
M_MAA_B7	AL18	SB_MA_7
M_MAA_B8	AN18	SB_MA_8
M_MAA_B9	AV17	SB_MA_9
M_MAA_B10	AK23	SB_MA_10
M_MAA_B11	AJ17	SB_MA_11
M_MAA_B12	AT18	SB_MA_12
M_MAA_B13	AK26	SB_MA_13
M_MAA_B14	AV15	SB_MA_14
M_MAA_B15	AV16	SB_MA_15
M_WE_B_N	AR25C	SB_WE#
M_CAS_B_N	AK25C	SB_CAS#
M_RAS_B_N	AP24C	SB_RAS#
M_SBS_B0	AP23	SB_BS_0
M_SBS_B1	AK24	SB_BS_1
M_SBS_B2	AW17	SB_BS_2
M_SCs_B_N0	AK25	SB_CS#_0
M_SCs_B_N1	AK25	SB_CS#_1
M_SCs_B_N0	AT25C	SB_CS#_2
M_SCs_B_N1	AT25C	SB_CS#_3
M_SCKE_B0	AV16	SB_CKE_0
M_SCKE_B1	AV15	SB_CKE_1
M_SCKE_B0	AV15	SB_CKE_3
M_ODT_B0	AL26	SB_ODT_0
M_ODT_B1	AP26	SB_ODT_1
M_ODT_B0	AK26	SB_ODT_2
M_ODT_B1	AK26	SB_ODT_3
CK_M_DDR0_B_DP	AL21	SB_CK_0
CK_M_DDR0_B_DN	AL22	SB_CK#_0
CK_M_DDR1_B_DP	AL20	SB_CK_1
CK_M_DDR1_B_DN	AK20	SB_CK#_1
CK_M_DDR0_B_DP	AK21	SB_CK_2
CK_M_DDR0_B_DN	AK21	SB_CK#_2
CK_M_DDR1_B_DP	AK21	SB_CK_3
CK_M_DDR1_B_DN	AK21	SB_CK#_3

SAN 100NF
(62-10055-441)

DDR3

<Variant Name>

wlstron

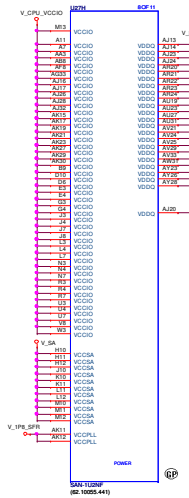
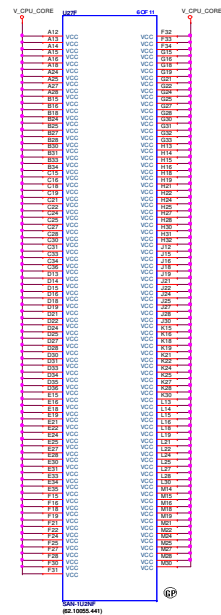
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Hsichih, Taipei

Part CPU LGA 1155_3

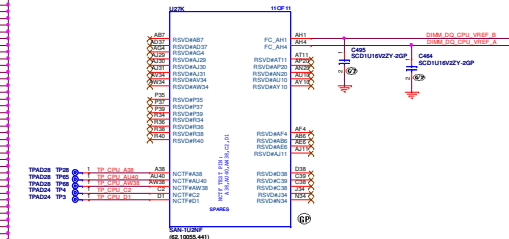
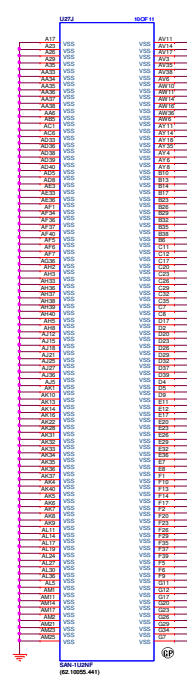
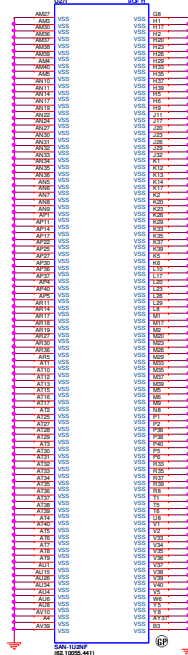
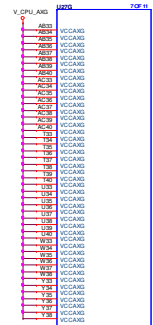
Size C Document Number New Mission Hills_MLK SA

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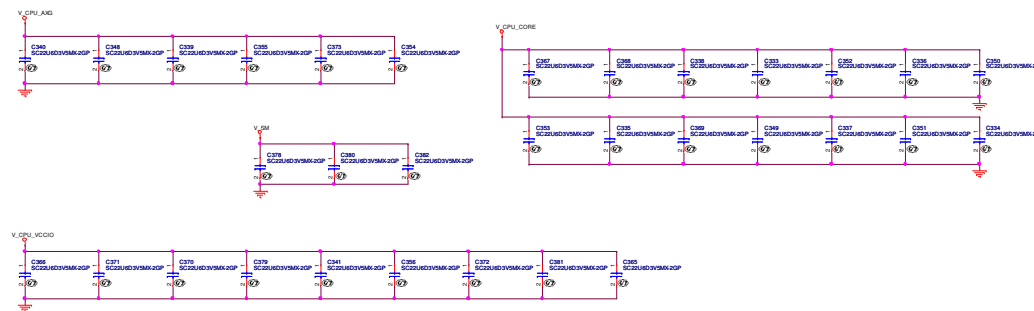
17 DIMM_Q0_CPU_VREF_B
18 DIMM_Q0_CPU_VREF_A



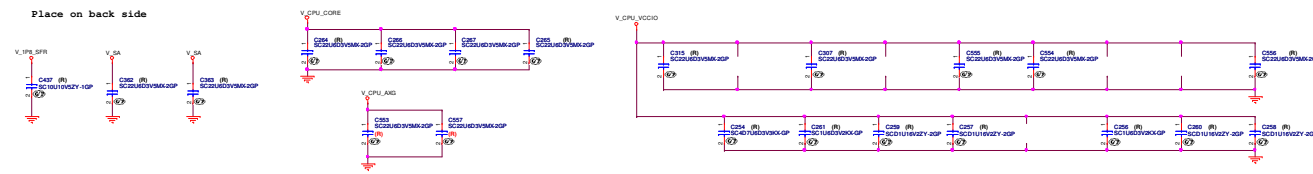
Net	CAP	AMOUNT
Vcore	22uf 0805	14+4
VCCIO	22uf 0805	9+16 (R)
V_AKG	22uf 0805	4+2 (R)
VCCSA	10uf 0805	2+0
VDDQ	22uf 0805	9
VCCPLL	10uf 0805	1



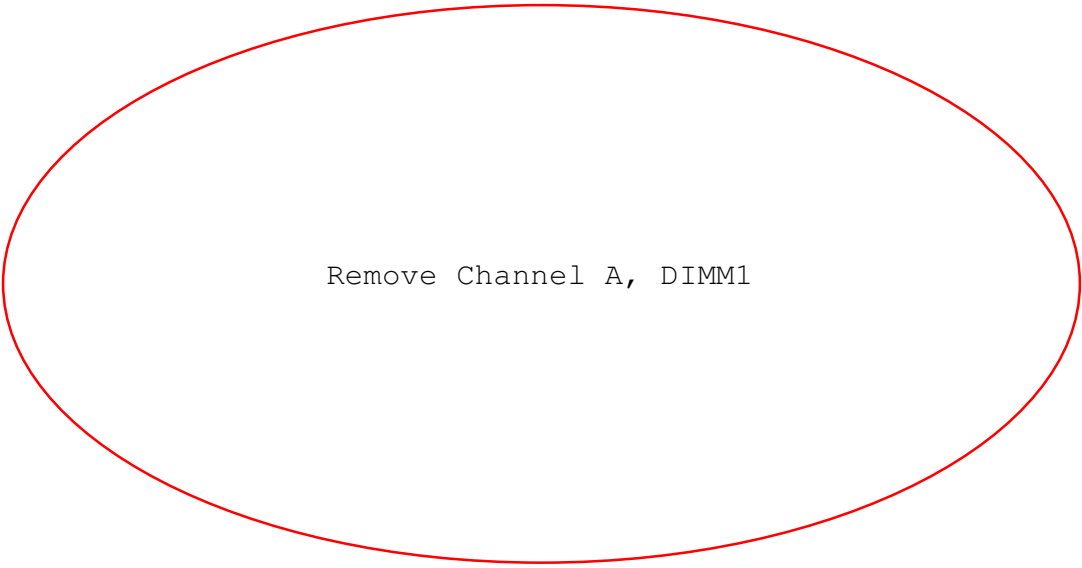
Place in the CPU Cavity Area



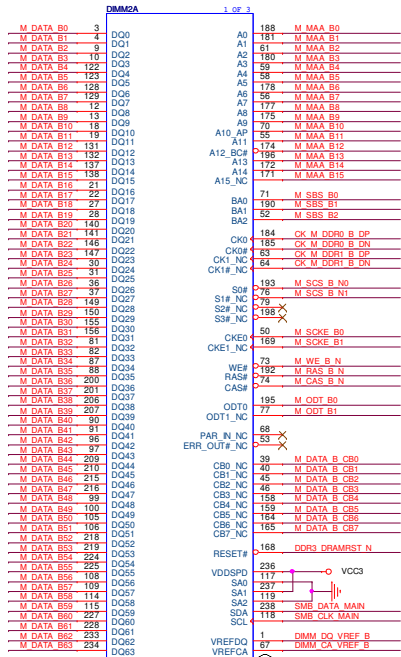
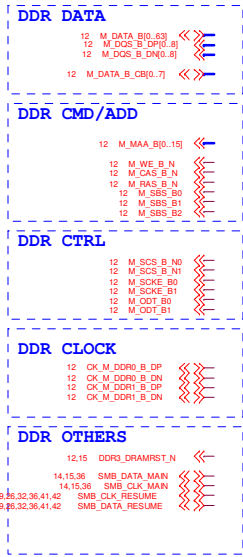
Place on back side



Notes:



Remove Channel A, DIMM1



DDR3 240P-4-GP
(22,10220,801)
Black color
Pin Height is 2.7mm

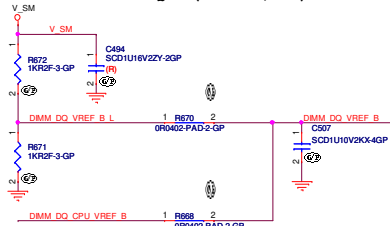
Trace: 12/12 mils

CHANNEL B DIMM1

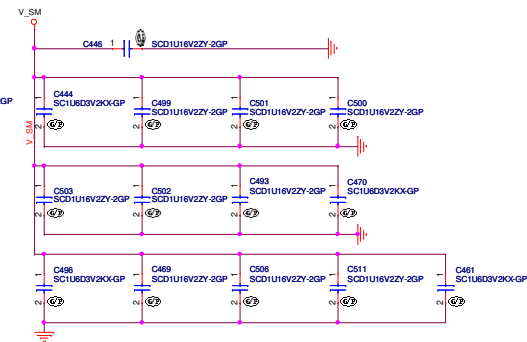
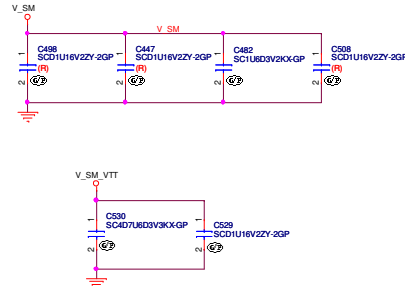
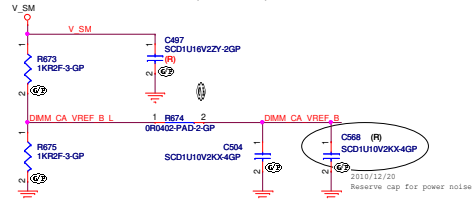
SMB ADDRESS: 010

SPD R/W: 0'A5, 0'A4

DIMM VREF DQ B (To DIMM/CPU)



DIMM VREF CA B (To DIMM)



<Variant Name>

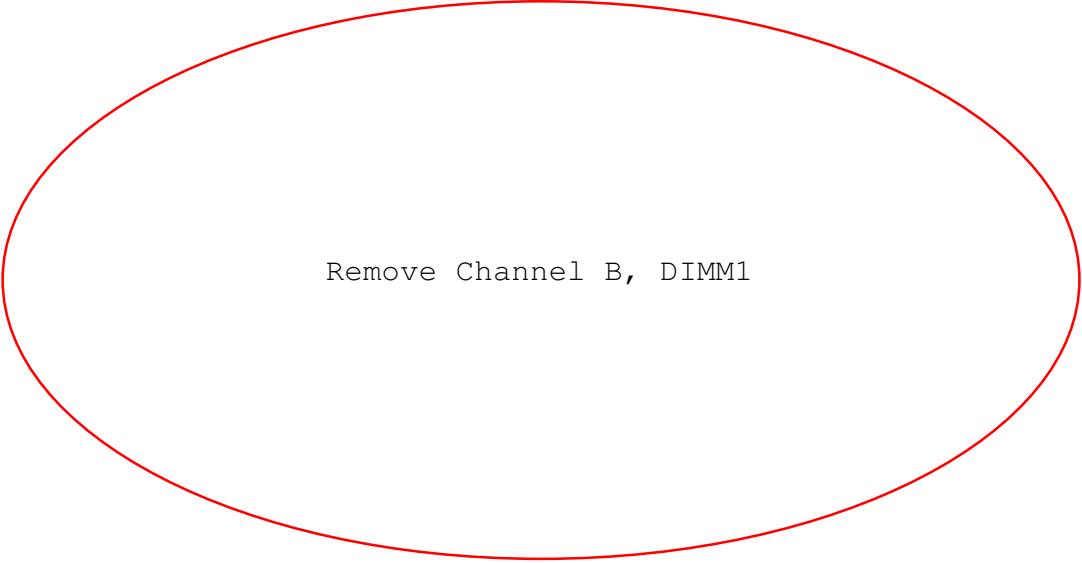
wlstron

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Hsichih, Taipei

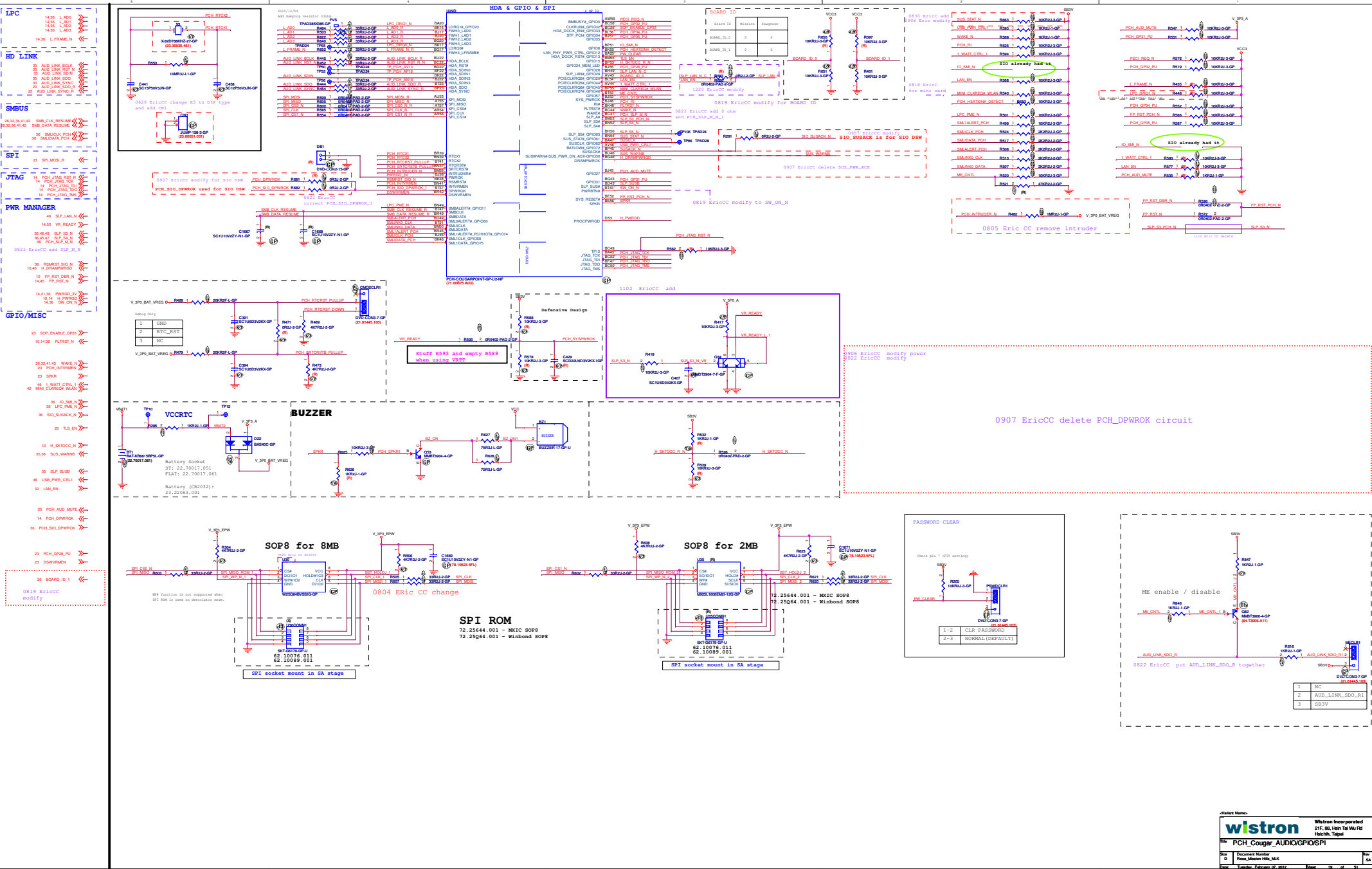
Title: **DDR3 CHB DIMM 0**

Size: C Document Number: Resa_Mission_His_MLK New SA

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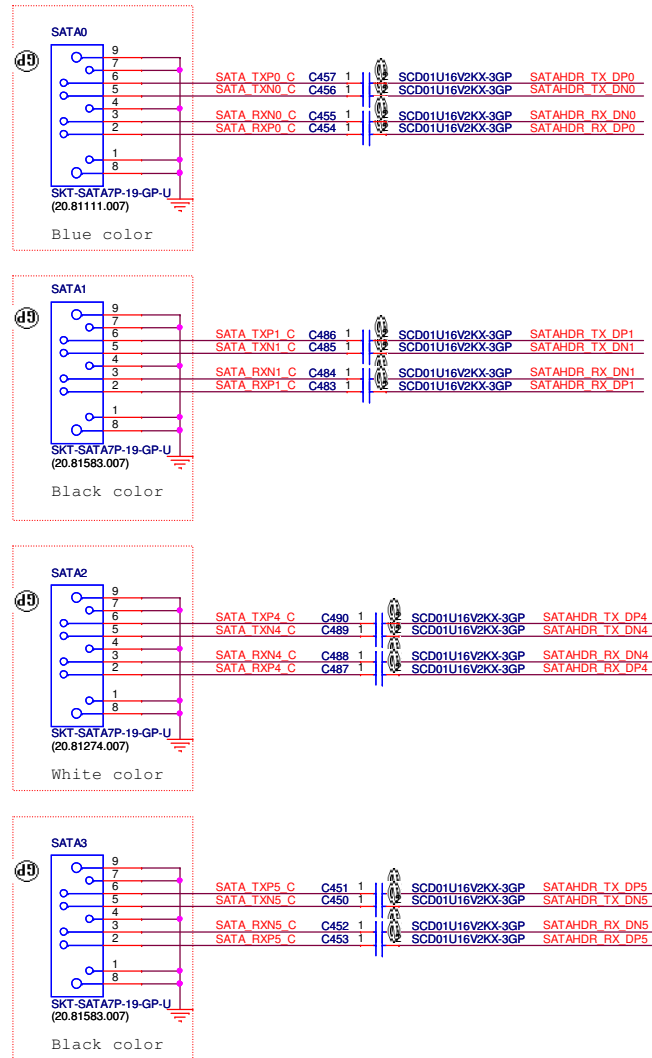


Remove Channel B, DIMM1



SATA

21	SATAHDR_RX_DP0	↔
21	SATAHDR_RX_DN0	↔
21	SATAHDR_TX_DN0	↔
21	SATAHDR_TX_DP0	↔
21	SATAHDR_RX_DP1	↔
21	SATAHDR_RX_DN1	↔
21	SATAHDR_TX_DN1	↔
21	SATAHDR_TX_DP1	↔
21	SATAHDR_RX_DP4	↔
21	SATAHDR_RX_DN4	↔
21	SATAHDR_TX_DN4	↔
21	SATAHDR_TX_DP4	↔
21	SATAHDR_RX_DP5	↔
21	SATAHDR_RX_DN5	↔
21	SATAHDR_TX_DN5	↔
21	SATAHDR_TX_DP5	↔



NOTE:

PCH only port 0&1 support SATA 3.0

<Variant Name>

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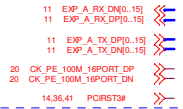
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Size A3 Document Number
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PCIEx16

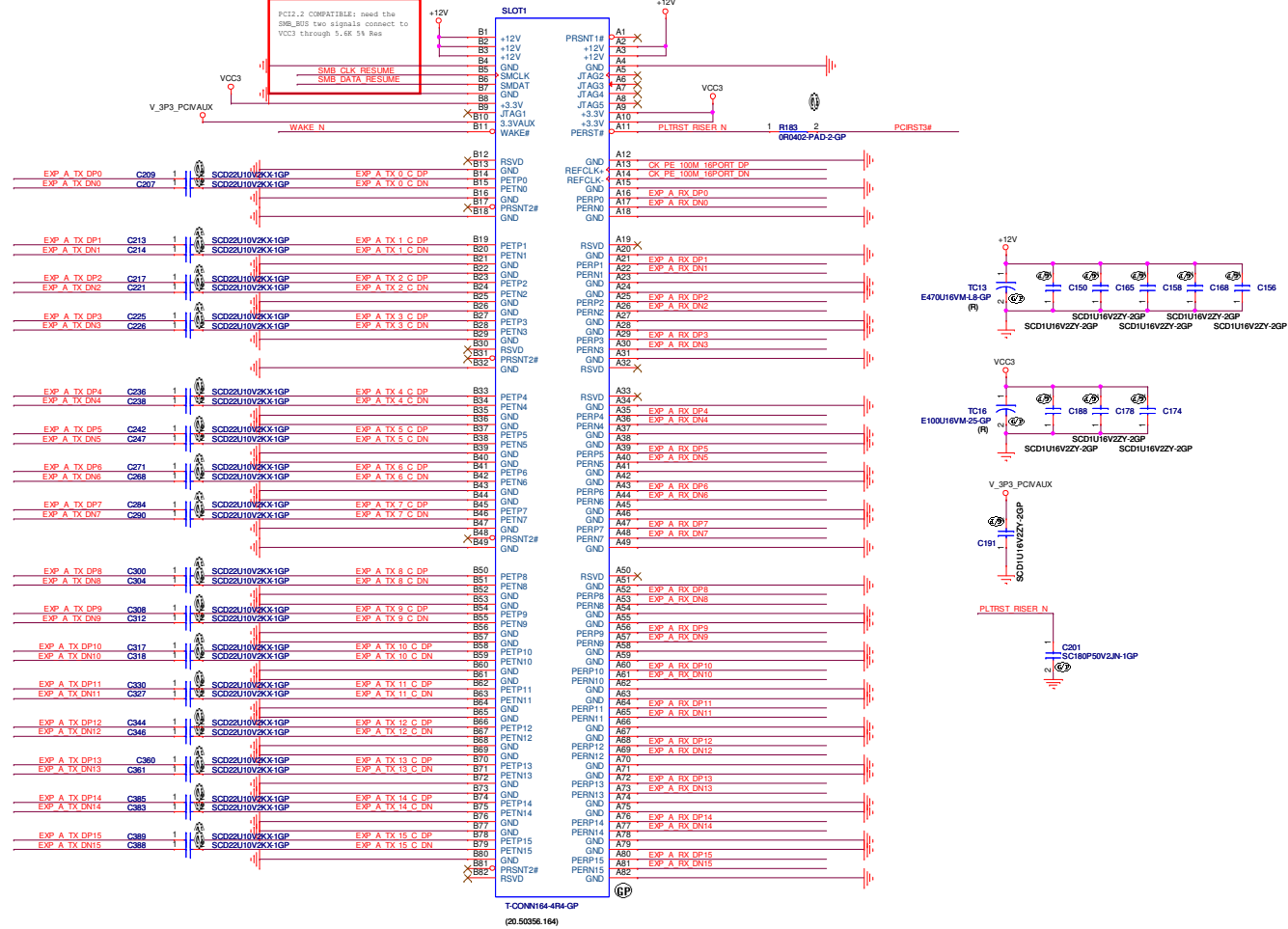


OTHERS



w/o Latch: 20.50352.164
with Latch: 20.50512.164, 20.50356.164

PCIEx16 CONN may need LATCH if supporting 75W GFX Card



<Variant Name>

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RGB

21 VGA_RED
21 VGA_GREEN
21 VGA_BLUE

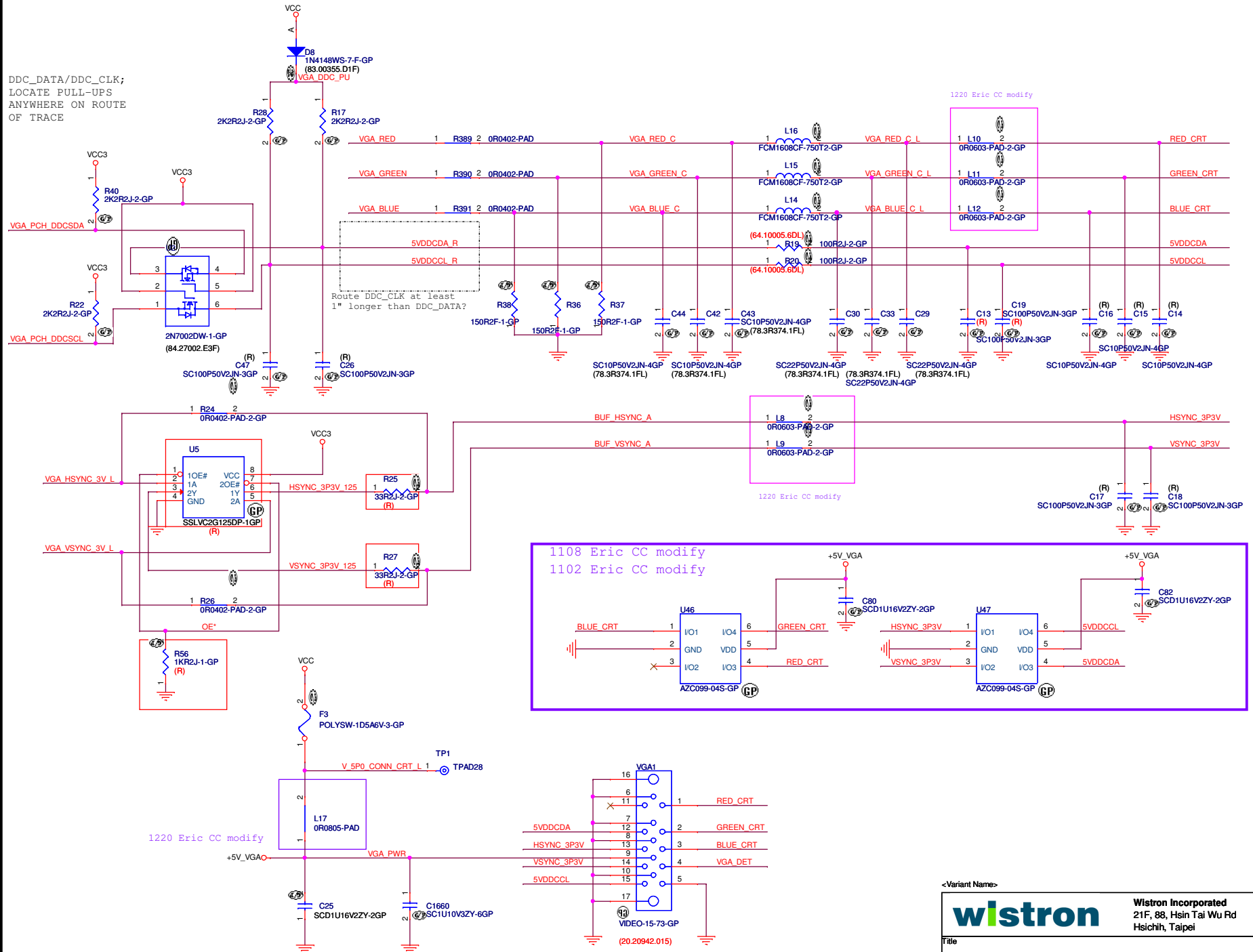
SYNC

21 VGA_HSYNC_3V_L
21 VGA_VSYNC_3V_L

DDC

21 VGA_PCH_DDCSDA
21 VGA_PCH_DDCSCL
21 VGA_DET

DDC_DATA/DDC_CLK;
LOCATE PULL-UPS
ANYWHERE ON ROUTE
OF TRACE



<Variant Name>

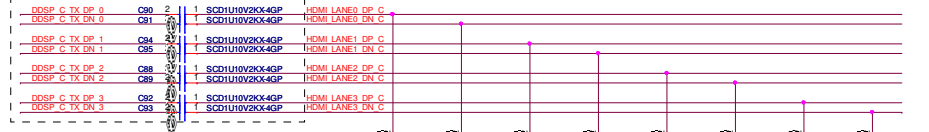
wistron			Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title			
Size A3	Document Number Rosa_Mission Hills_MLK		Rev SA
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HDMI PORT

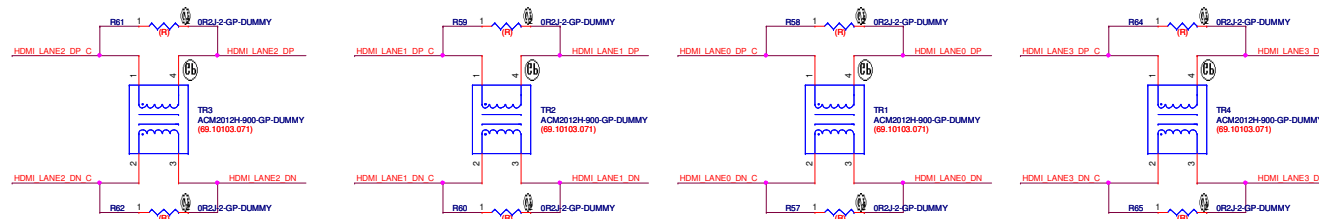
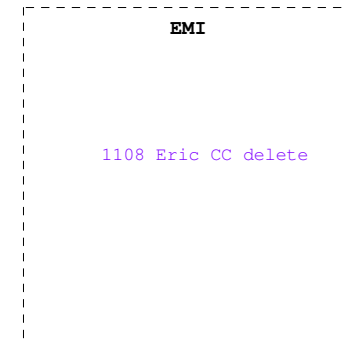
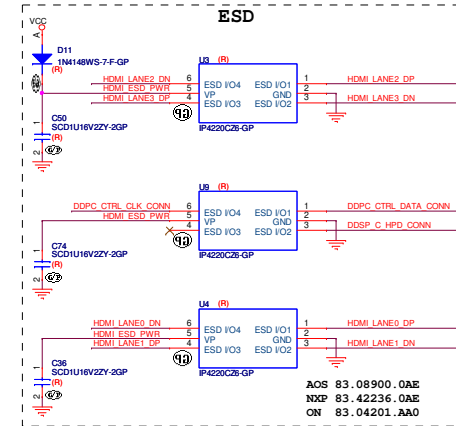
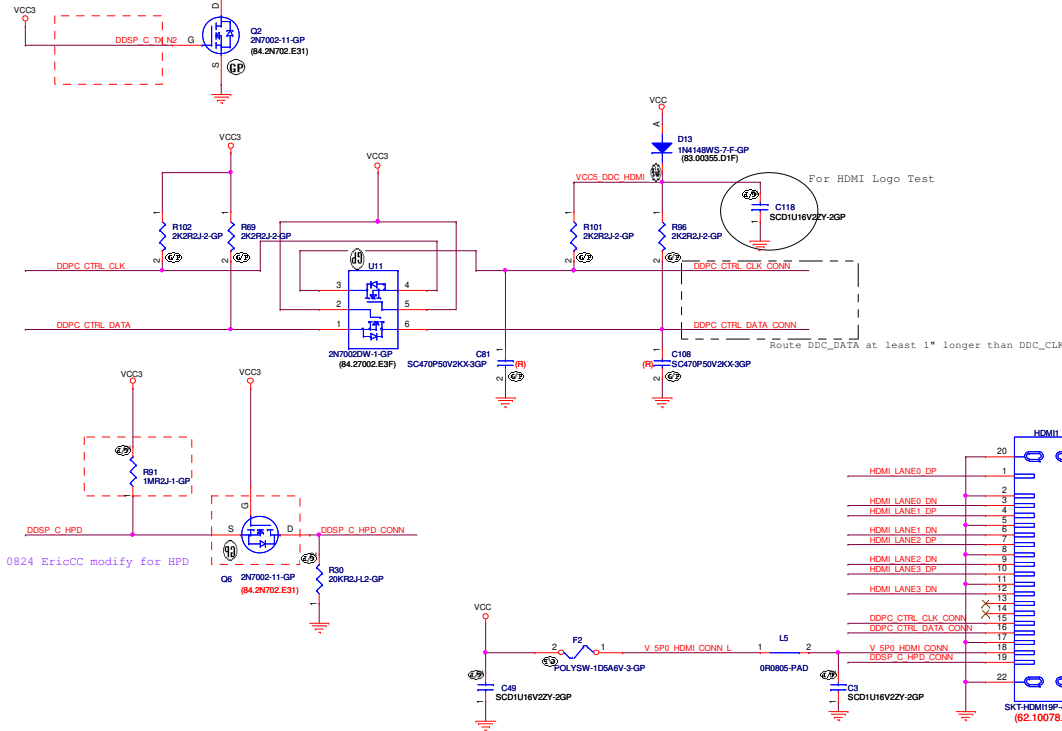
21 DDSP_C_TX_DP_0
21 DDSP_C_TX_DN_0
21 DDSP_C_TX_DP_1
21 DDSP_C_TX_DN_1
21 DDSP_C_TX_DP_2
21 DDSP_C_TX_DN_2
21 DDSP_C_TX_DP_3
21 DDSP_C_TX_DN_3
21 DDPC_CTRL_CLK
21 DDPC_CTRL_DATA
21 DDSP_C_HPD

0824 ERIC CC change NET NAME from port D to C

PCH PORT C Place near HDMI Connector



0830 ERIC CC delete R39 and R66



<Variant Name>

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Hsinchu, Taipei

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DISPLAY PORT

RESERVED

<Variant Name>

wistron

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Hsinchu, Taipei

Title

Size
C

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FRONT USB

22 USB_PCH_DP8
22 USB_PCH_DN8
22 USB_PCH_DP9
22 USB_PCH_DN9

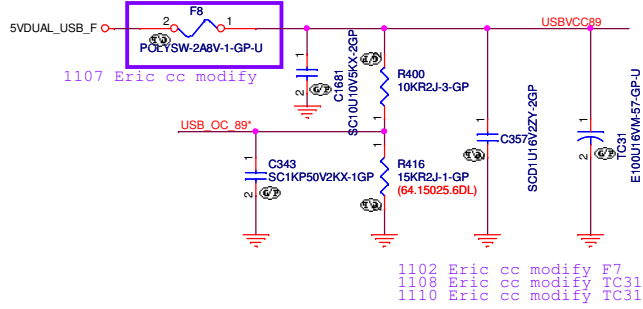
22 USB_OC_89*
21 FB_USBF1_DET

22 USB_PCH_DP10
22 USB_PCH_DN10
22 USB_PCH_DP11
22 USB_PCH_DN11

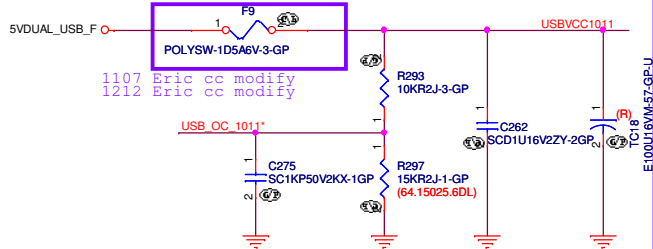
22 USB_OC_1011*
21 FB_USBF2_DET

0819 Eric CC modify for USB3.0 mapping

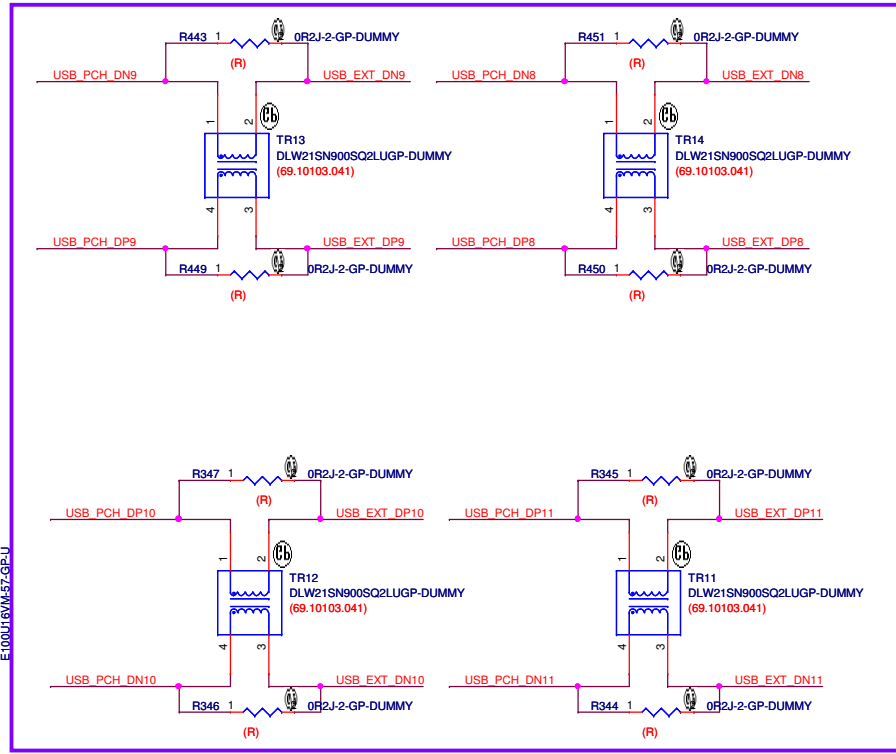
FRONT USB PORT GREEN



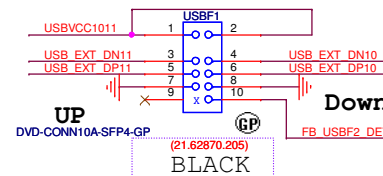
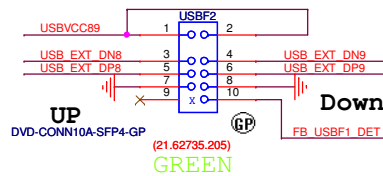
FRONT USB PORT BLACK



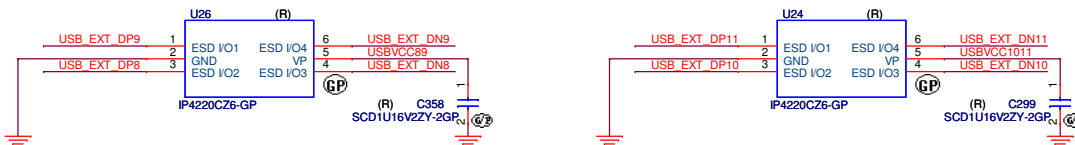
1101 Eric cc modify F7
0908 modify F7
0901 Eric CC modify net name for layout



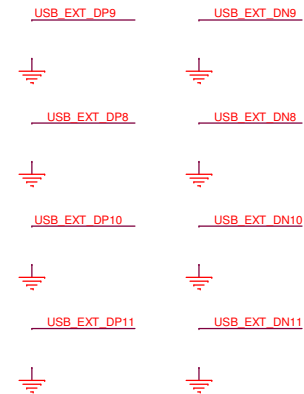
USB CONNECTOR



ESD



EMI



<Variant Name>

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Hsichih, Taipei

Title

Size Document Number Rev
CustomRosa_Mission Hills_MLK SA

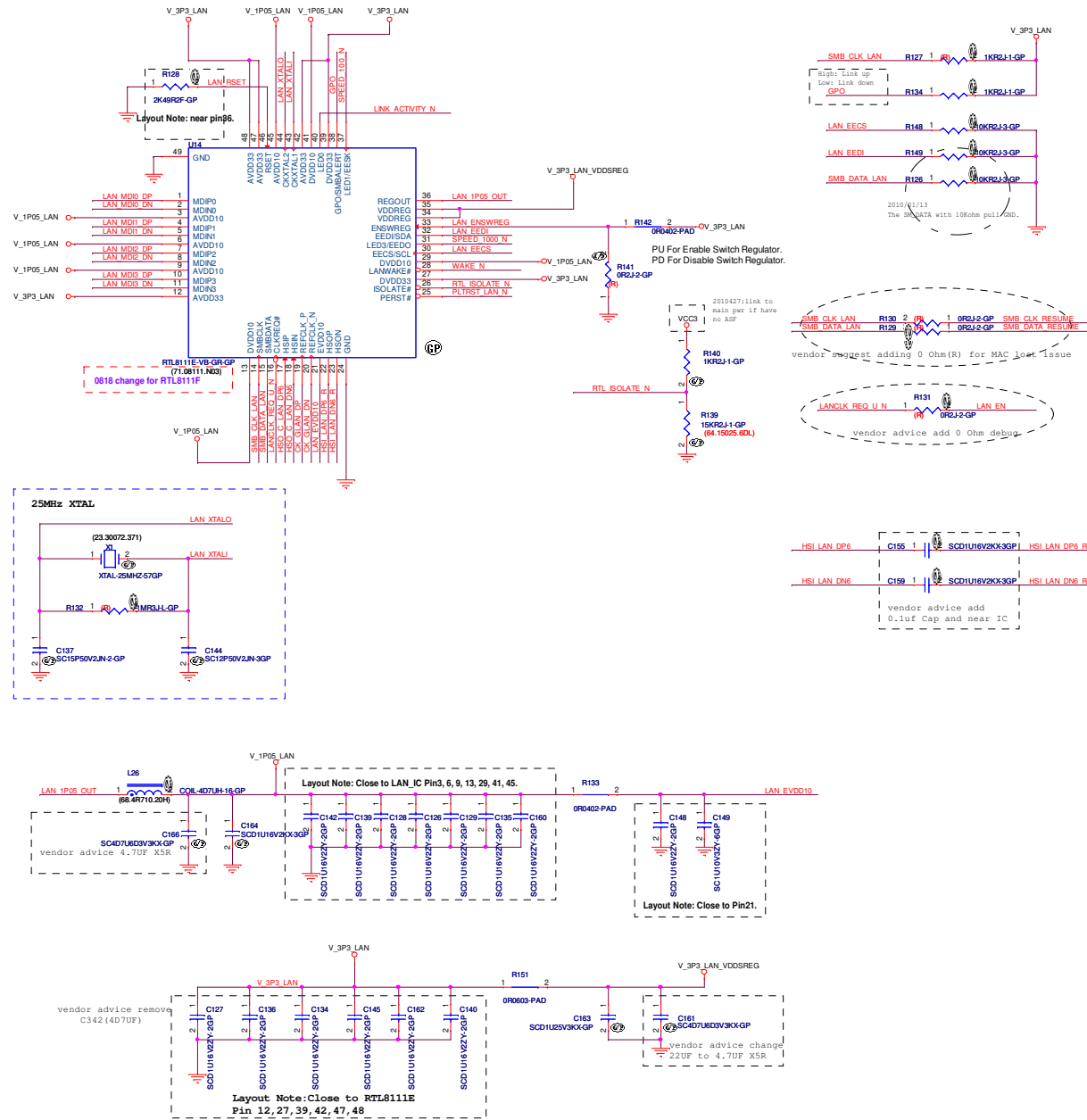
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To connector

31 LAN_MDIO_DP
31 LAN_MDIO_DN
31 LAN_MDIO_DP
31 LAN_MDIO_DN
31 LAN_MDIO_DP
31 LAN_MDIO_DN
31 LAN_MDIO_DP
31 LAN_MDIO_DN
31 SPEED_100_N
31 SPEED_1000_N
31 LINK_ACTIVITY_N

OTHERS

20 CK_GLAN_DP
20 CK_GLAN_DN
22 HSI_LAN_DP6
22 HSI_LAN_DN6
22 HSO_C_LAN_DP6
22 HSO_C_LAN_DN6
19,26,36,41,42 SMB_CLK_RESUME
19,26,36,41,42 SMB_DATA_RESUME
19 LAN_EN
36,42 PLTRST_LAN_N
19,26,41,42 WAKE_N



<Variant Name>

wistron

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Hsichih, Taipei

Title

Size

C

Document Number

Pass_Mission Hills MLK

Rev

SA

Date

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HD_LINK

19 AUD_LINK_SDN
19 AUD_LINK_SDO
19 AUD_LINK_RST_N
19 AUD_LINK_SYNC
19 AUD_LINK_BCLK

AUDIO RAER PORT

Line-in
34 LIN_L
34 LIN_R
34 LIN_ID

MIC-IN

34 MIC_IN_L
34 MIC_IN_R
34 MIC_VREF0
34 MIC_ID

Line-out

34 LOUT_L
34 LOUT_R
34 LOUT_ID

Front I/O

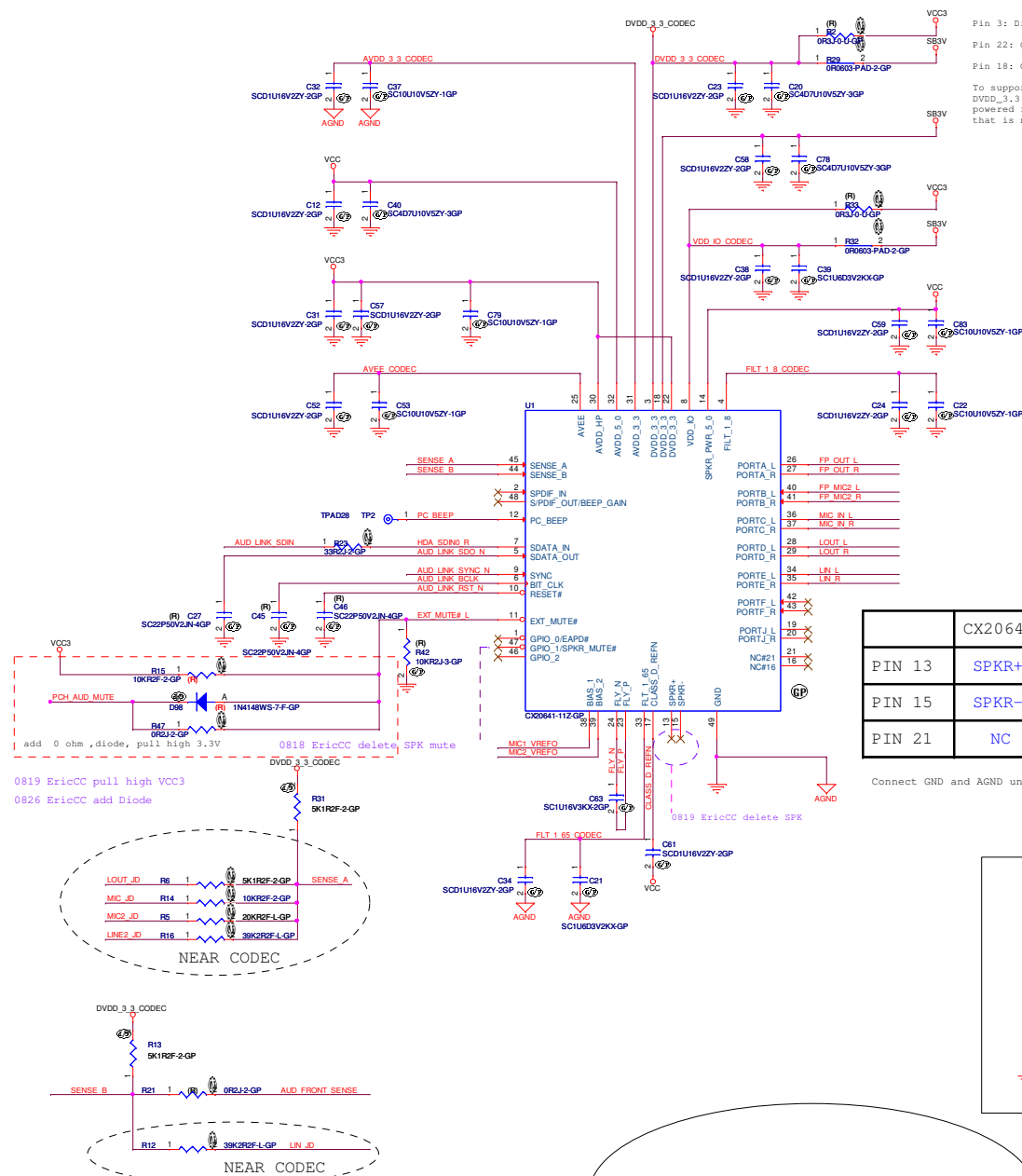
MIC-IN
34 FP_MIC2_R
34 FP_MIC2_L
34 MIC2_ID
34 MIC2_VREF0

HP-OUT

34 FP_OUT_L
34 FP_OUT_R
34 LINE2_ID

MISC

34 AUD_FRONT_SENSE
19 PCH_AUD_MUTE



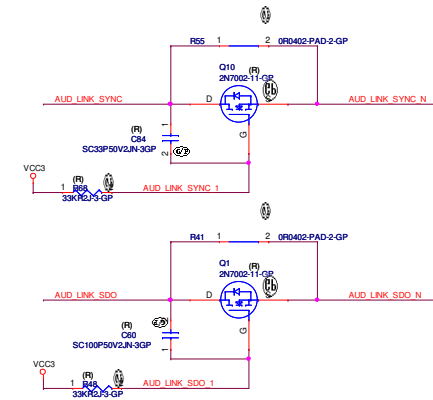
Pin 3: Digital Supply Voltage 3.3V

Pin 22: Charge Pump Input 3.3V

Pin 18: Class-D Supply 3.3V

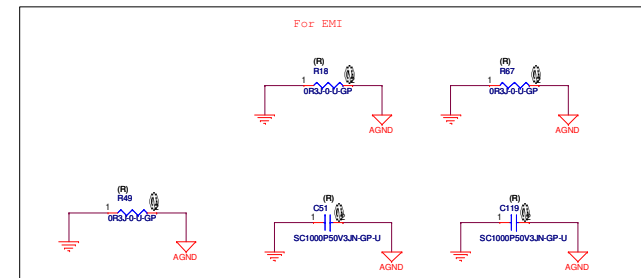
To support Wake-On-Jack Functionality, DVDD_3.3 and VDD_IO should be powered from a power supply that is never removed

	CX20641/CX20651	
Line-in	pin34/35	Port E
Line-out	pin28/29	Port D
Mic-in-R	pin36/37	Port C
Mic-in-F	pin40/41	Port B
HP-out	pin26/27	Port A



	CX20641	CX20651
PIN 13	SPKR+	NC
PIN 15	SPKR-	NC
PIN 21	NC	PORT I

Connect GND and AGND under Codec



Remove De-Pop Circuit

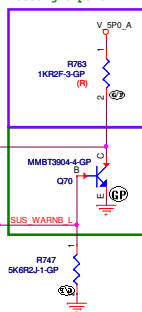
0907 EricCC Modify for SIO DSW
0819 EricCC Modify

19,36 SUS_WARNB >>
19 SLP_SUSB >>
48 SLP_SUS_FET <<
46 SUS_WARN_SVDUAL <<

If use PCH DSW, the green rectangle part
are Unmount (R)

S0	S3	S5	DS
L	L	L	H

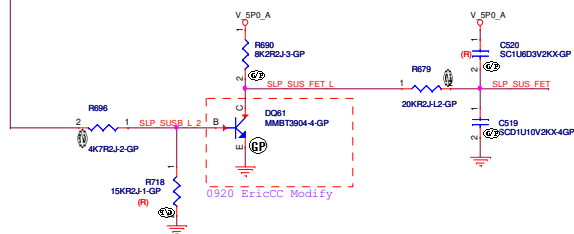
S0	S3	S5	DS
H	H	H	L



1213 Eric add

S0	S3	S5	DS
H	H	H	L

SLP_SUSB



0920 EricCC Modify

S0	S3	S5	DS
L	L	L	H

<Variant Name>

wistron

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Hsichih, Taipei

Title DSW

Size C Document Number
Pesa_Mission_Hills_MLK

Rev
SA

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PS2 KB/MS

0920 EricCC delete

<Variant Name>

wistron

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
KBMS

Size A4 Document Number
Rosa_Mission Hills MLK

Rev
SA

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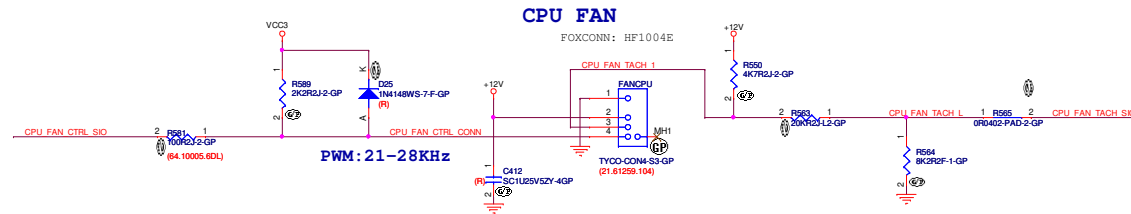


SIO FAN CONTROL

36 CPU_FAN_CTRL_SIO
36 CPU_FAN_TACH_SIO

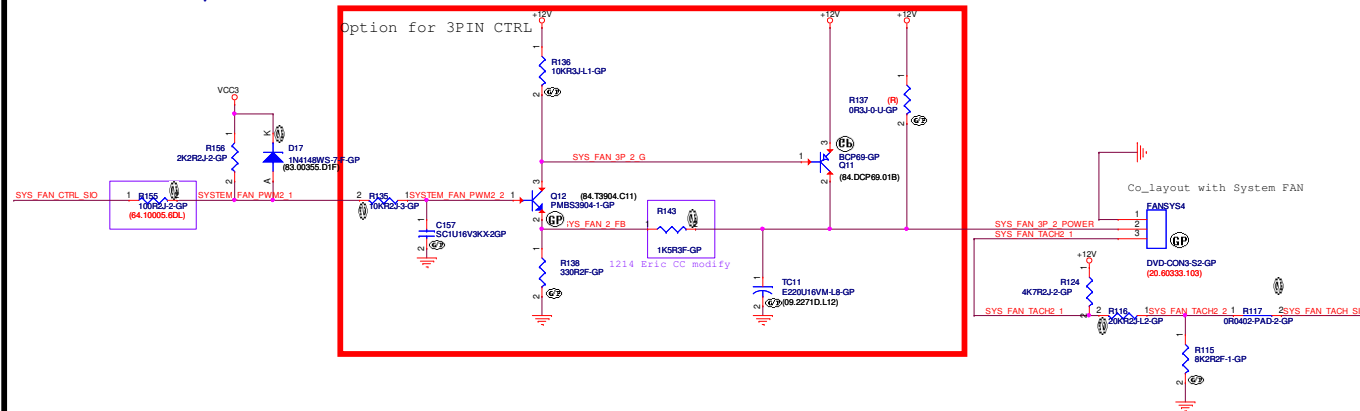
36 SYS_FAN_CTRL_SIO
36 SYS_FAN_TACH_SIO

0805 Eric CC delete for
FANSYS1 Circuit

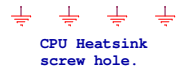


0805 Eric CC remove FANSYS1 Circuit

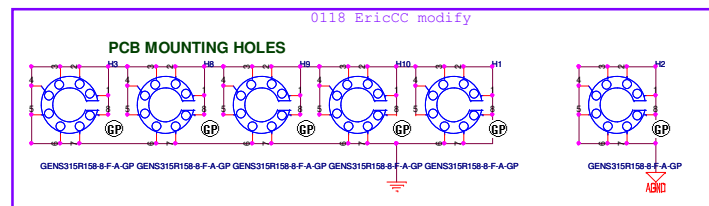
2nd SYS 3 PINS/4 PINS FAN CONTROL



Remove CPU Heatsink Screw Holes



CPU Heatsink
screw hole.



Variant Name:

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File: FAN CIRCUITS/HOLE


Size: Document Number
Customer: Mission Hills MLK

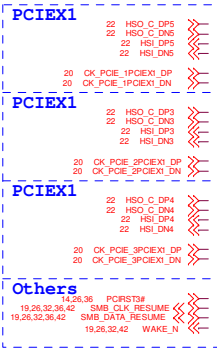
Rev
SA

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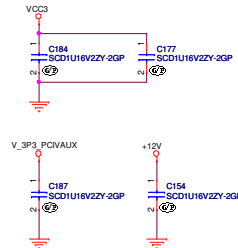
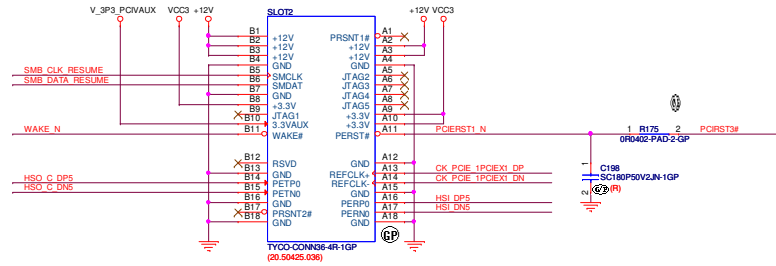
5					4					3					2					1																								
D																																												
C																																												
B																																												
A																																												
5					4					3					2					1																								



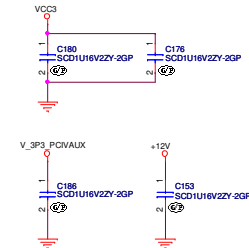
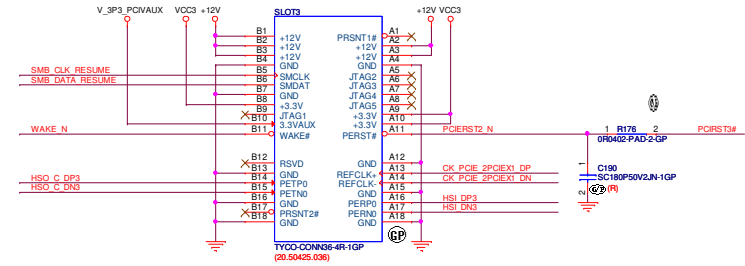
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		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
Size B	Document Number Rosa_Mission Hills MLK		Rev SA
Date:	Tuesday, February 07, 2012	Sheet	40 of 51



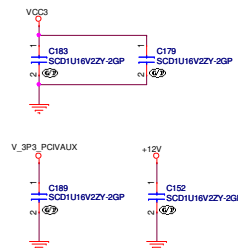
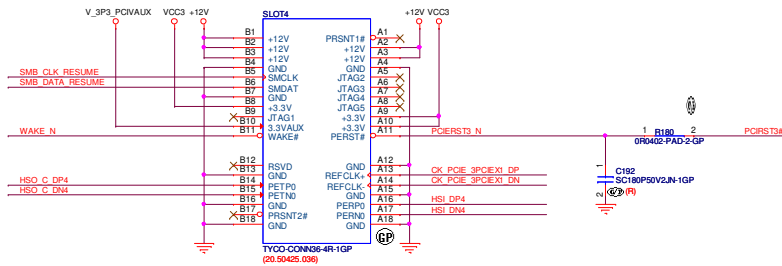
PCIEX1 CONN



PCIEX1 CONN



PCIEX1 CONN



<Variant Name>

wistron Wistron Incorporated
21F, 88, Hei Tai Wu Rd
Hsichih, Taipei

Title PCIEX1 CONN

Size C

Document Number
Pesa_Mission Hills MLK

Rev SA

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Wireless Card(Present support EP/SP)

USB2.0

22 USB_PCH_DP12
22 USB_PCH_DN12

PCIEX1

22 HSO_C_DP2
22 HSO_C_DN2
22 HSI_DP2
22 HSI_DN2
20 CK_PCIEX1_WLAN_DP
20 CK_PCIEX1_WLAN_DN

OTHERS

19,26,32,36,41 SMB_CLK_RESUME
19,26,32,36,41 SMB_DATA_RESUME

19,26,32,41 WAKE_N
32,36 PLTRST_LAN_N

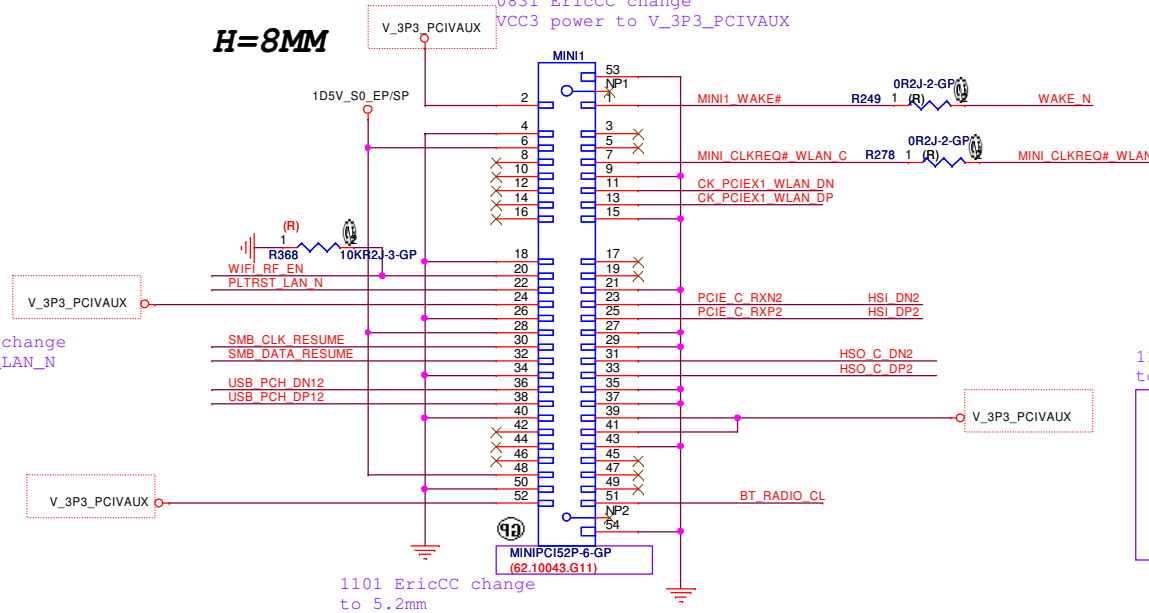
19 MINI_CLKREQ#_WLAN
20 WIFI_RF_EN

20 BT_RADIO_CL

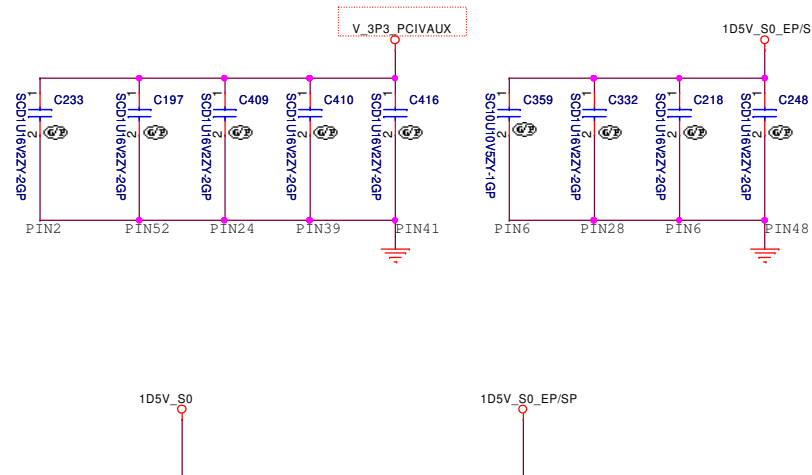
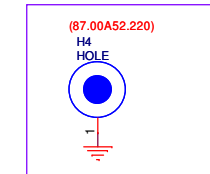
0826 EricCC change
for PLTRST_LAN_N

H=8MM

0831 EricCC change
VCC3 power to V_3P3_PCIVAUX



1101 EricCC change standoff
to 5.2mm



<Variant Name>

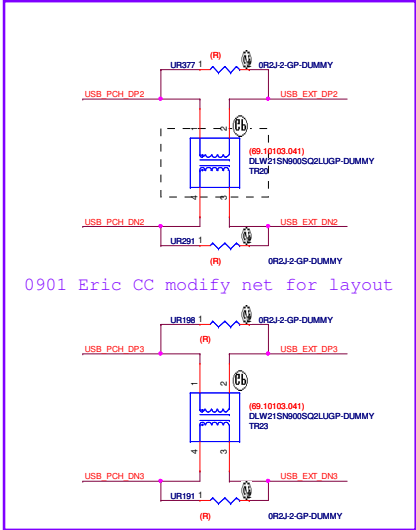
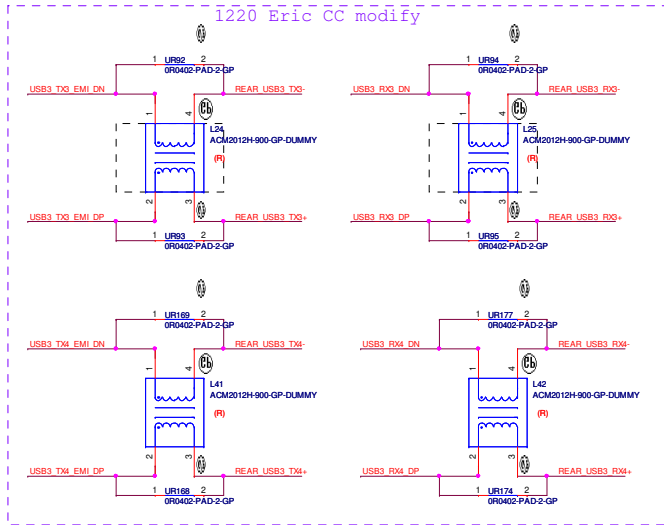
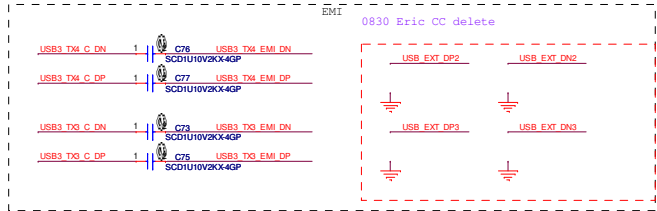
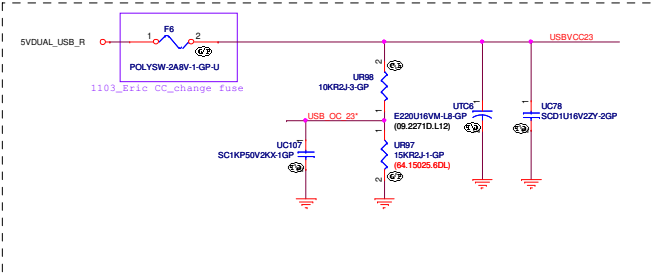
wistron			Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Mini PCIe Slot			
Title Size B	Document Number Rosa_Mission Hills MLK	Rev SA	
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Rear USB3.0

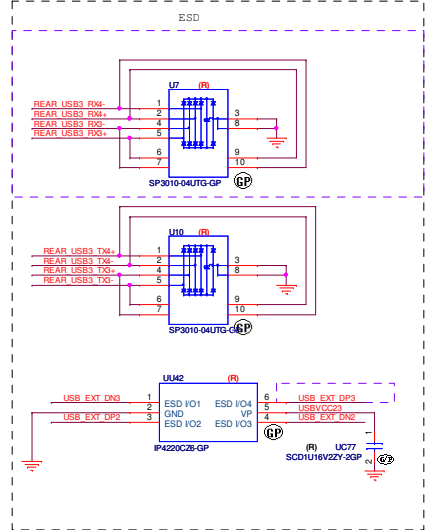
- 20 USB3_RXQ_DN
- 20 USB3_RXQ_DP
- 20 USB3_TXQ_C_DN
- 20 USB3_TXQ_C_DP
- 20 USB3_RX4_DN
- 20 USB3_RX4_DP
- 20 USB3_TX4_C_DN
- 20 USB3_TX4_C_DP
- 22 USB_PCH_DP2
- 22 USB_PCH_DN2
- 22 USB_PCH_DP3
- 22 USB_PCH_DN3
- 22 USB_OC_23*

0819 Eric CC modify placement for USB3.0

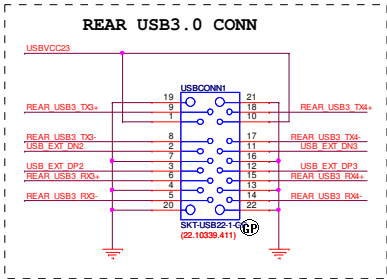
REAR USB3.0

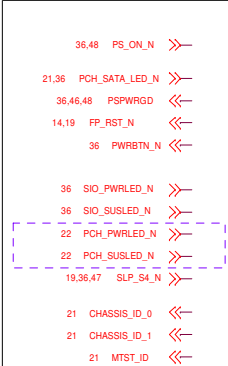


0901 Eric CC modify net for layout

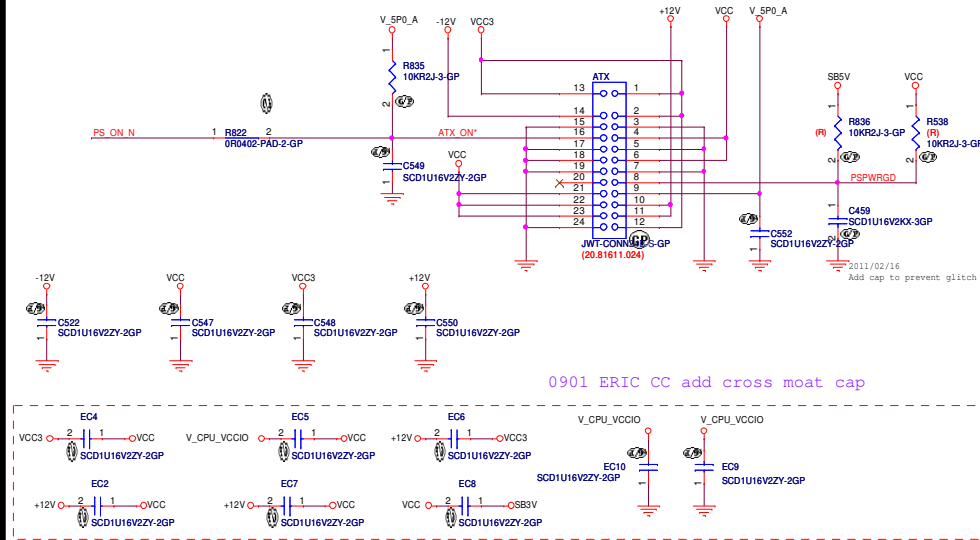


0902 Eric CC modify F7





ATX CONNECTOR



0815 ERIC CC MODIFY

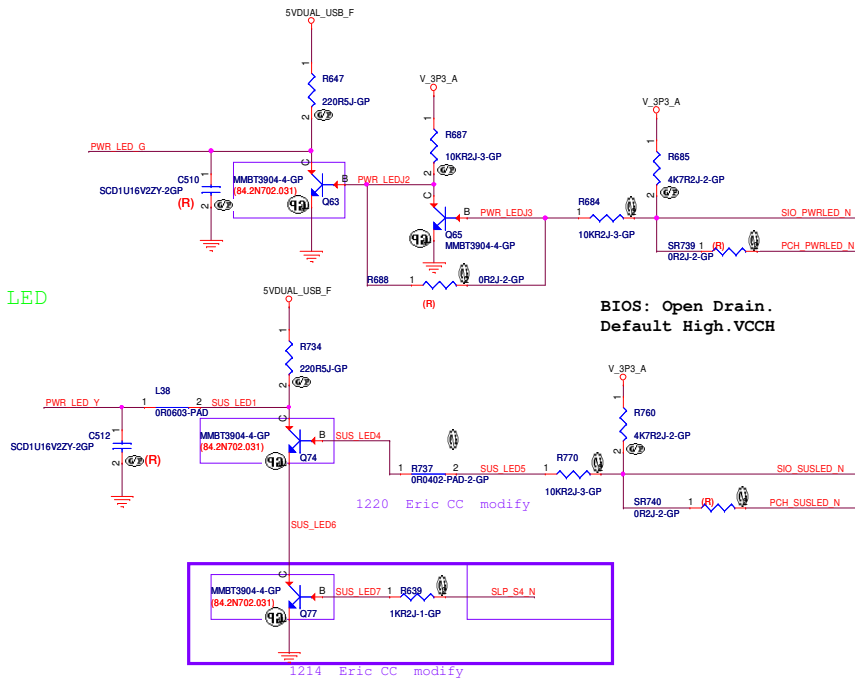
Amber LED



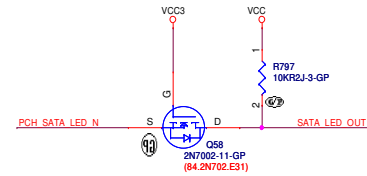
Green LED



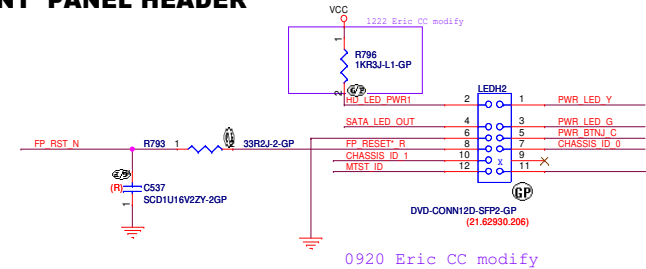
S0	White
S3	Amber
S4	LED off
No Post	Amber
Failure to Post	Amber (blinking)



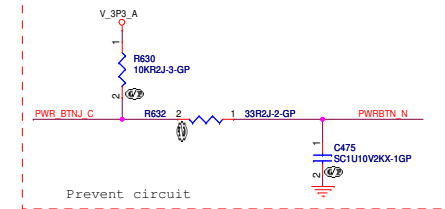
HDD LED



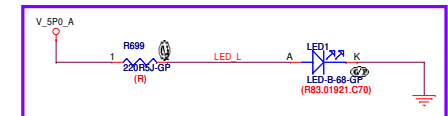
FRONT PANEL HEADER



POWER BUTTON



1101 Eric CC remove LED



<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title		PWR/FNT PNL	
Size	Document Number	Rev	
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0824 ERIC CC change POWER circuit

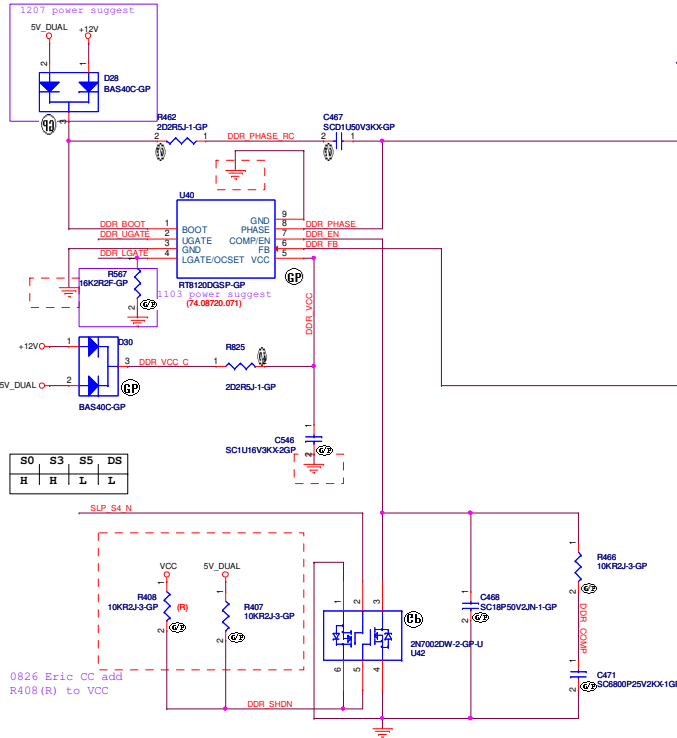
0805 Eric CC change
for U40

0823 Eric CC change
for GND

$$V_{out} = 0.8V(1+R1/R2)$$

$$I_{peak} = (40\mu A \cdot R_{ocset} - 0.4V) / R_{dson}$$

$$R_{ocset} = 13.3K, R_{dson} = 5.5m\Omega, I_{peak} = 24A$$



84.03004.036 QM3004D
Vgs @ 4.5V,
Id = 55A,
Rds(on) = 11~14mohm,

84.03006.036 QM3006D
Vgs @ 4.5V,
Id = 78A,
Rds(on) = 7.5~9mohm,

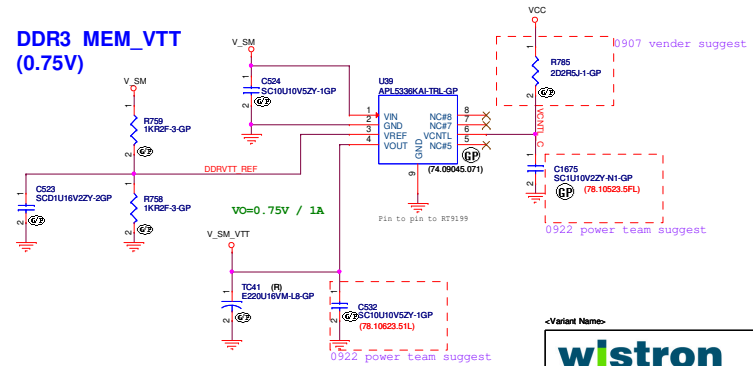
VIN RIPLE CURRENT Imax=7.79A

Iomax=17.0A
OCP>25.5A

1108 Eric CC delete
0922 power team suggest

Please put above 1st DIMM slot

DDR3 MEM_VTT (0.75V)



<Variant Name>

wlstron

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Hsichih, Taipei

Title DDR POWER

Size C Document Number Pss_Mission_His_MLK New SA

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VCC5A/VCC3A

SB5V/SB3V

V_3P3_A 1.5A

$1.25 \times (R1+R2)/R1 = 3.3V$

0824 ERIC CC add

2010/12/17
Change R762 from 9402 to 0603 size

1.8V/1.5A

$1.25 \times (R1+R2)/R1 = 1.8V$

0824 ERIC CC add
1103 power team suggest

V_1P05_PCH

Remove optional ME Power
since it is tied with PCH Power

0823 EricCC
change to 7.5kohms

0823 EricCC delete

V_3P3_DAC_FB_R

0823 EricCC delete

0823 ERIC CC change F7
0824 ERIC CC remove F7

Stuff TC26 when use L31

V_1P5 0823 EricCC add for Mini card Power
0824 EricCC modify for MOS

IDmax = 0.75A
For Mini-PCIE

0830 EricCC add R667
0826 EricCC modify net name

0826 EricCC modify
C227 F7

1104 EricCC delete ME power

0824 EricCC Revserve

STUFF MR18 FOR NON AMT

<Variant Name>

wlstron

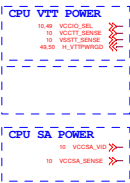
Wistron Incorporated
21F, 88, Hein Tai Wu Rd
Hsichih, Taipei

Title SYSTEM POWER

Size C Document Number
Pss_Mission_His_MLK

Rev SA

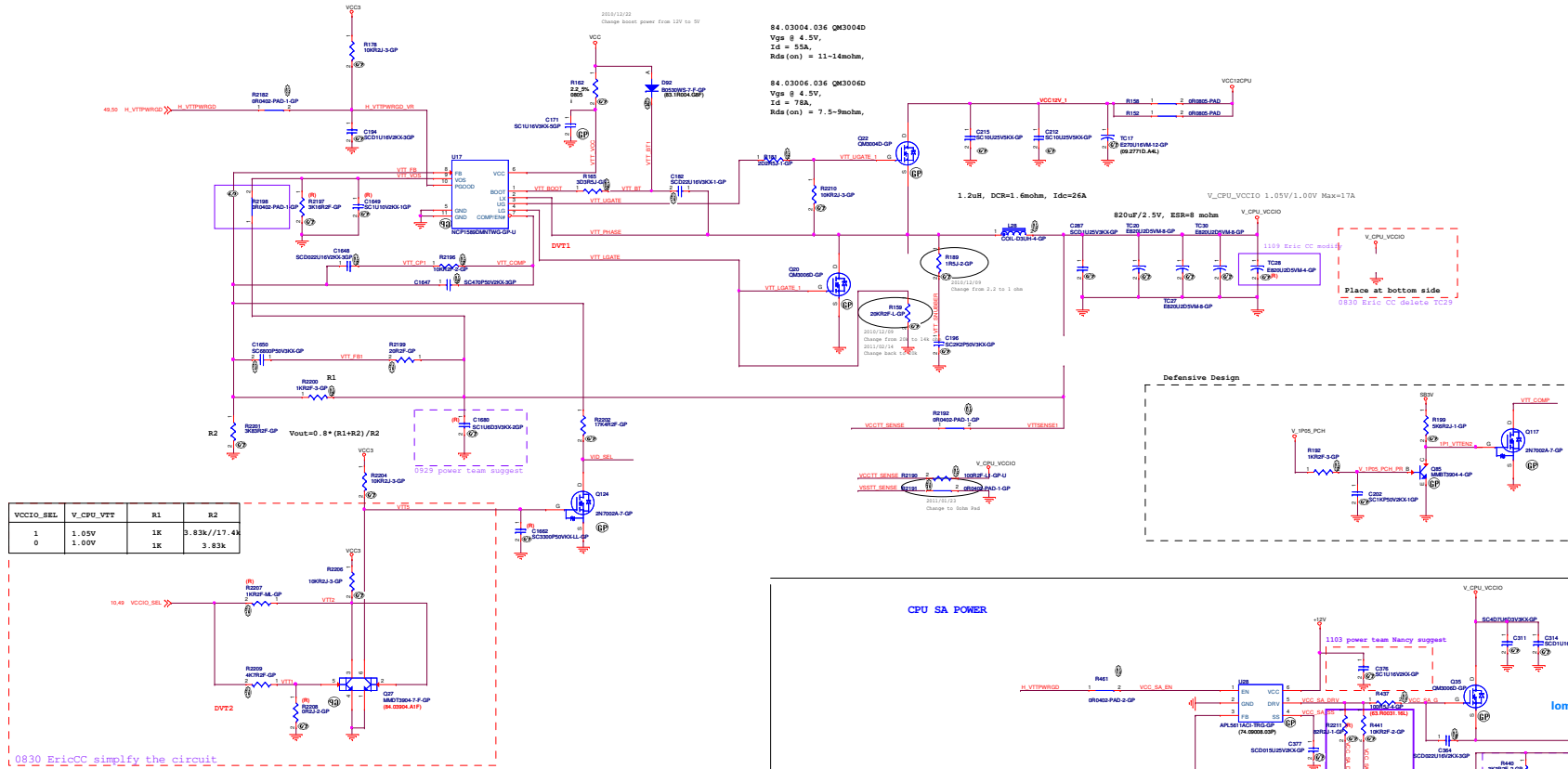
Date: Tuesday, February 07, 2012 Sheet 48 of 51



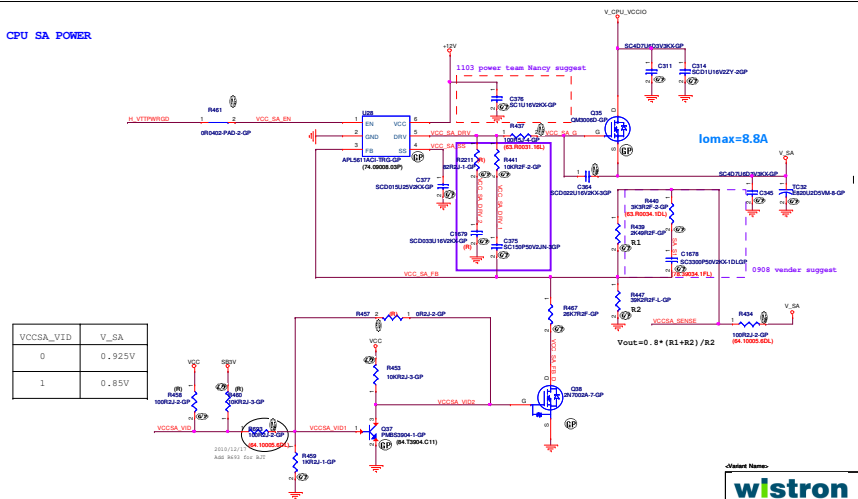
CPU VTT POWER

$I_{peak} = (8.5\mu A \cdot R_{ocset}) / (DCR \cdot K)$

$R_{ocset} = 6.49K, DCR = 1.6m\Omega, K = 1.3, I_{peak} = 26.5A$



CPU SA POWER



```

49  H_VTTPWRIGD  >>>
10  VCC_SENSE   >>>
10  VSS_SENSE   >>>
10  H_VIDOUT_VR >>>
10  H_VIDSCK_VR >>>
10  H_VIDALERT_VR >>>

50.51 PWM0     <<<
50.51 CSN1     <<<
50.51 CSPI     <<<

50.51 PWM2     <<<
50.51 CSN2     <<<
50.51 CSPI2    <<<

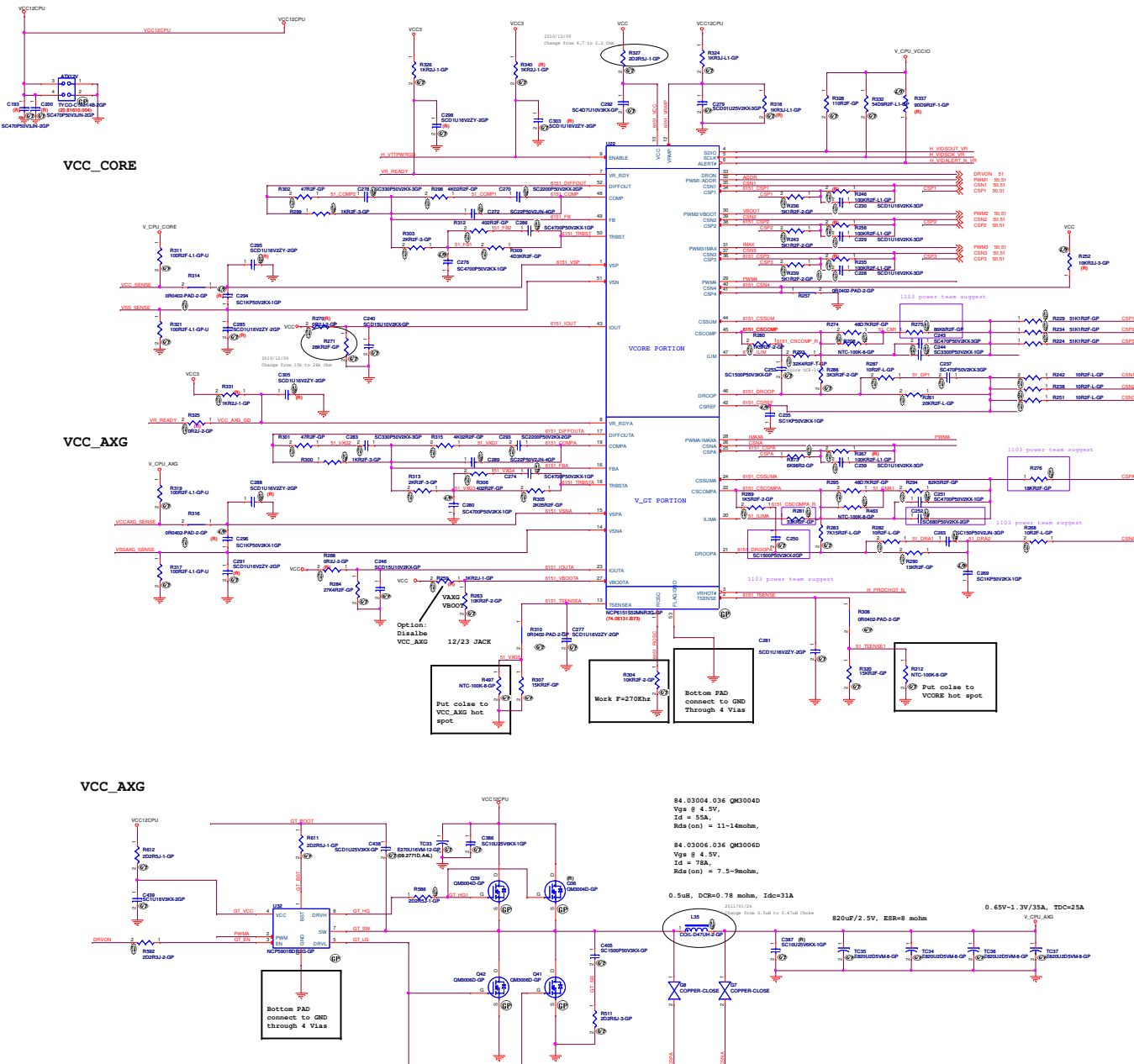
50.51 PWM3     <<<
50.51 CSN3     <<<
50.51 CSPI3    <<<

14.19 VR_READY <<<

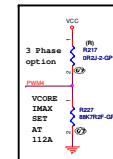
```

10 VCCAQ_SENSE

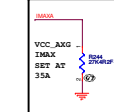
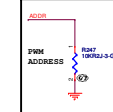
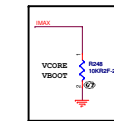
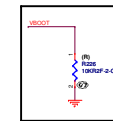
10 H_PROCHOT_N <<-



PWM ADDRESS		
Resistor value	SVID address for Vcore rail	SVID address for VCC_AXG rail
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
124K	1010	1011
165K	1100	1101



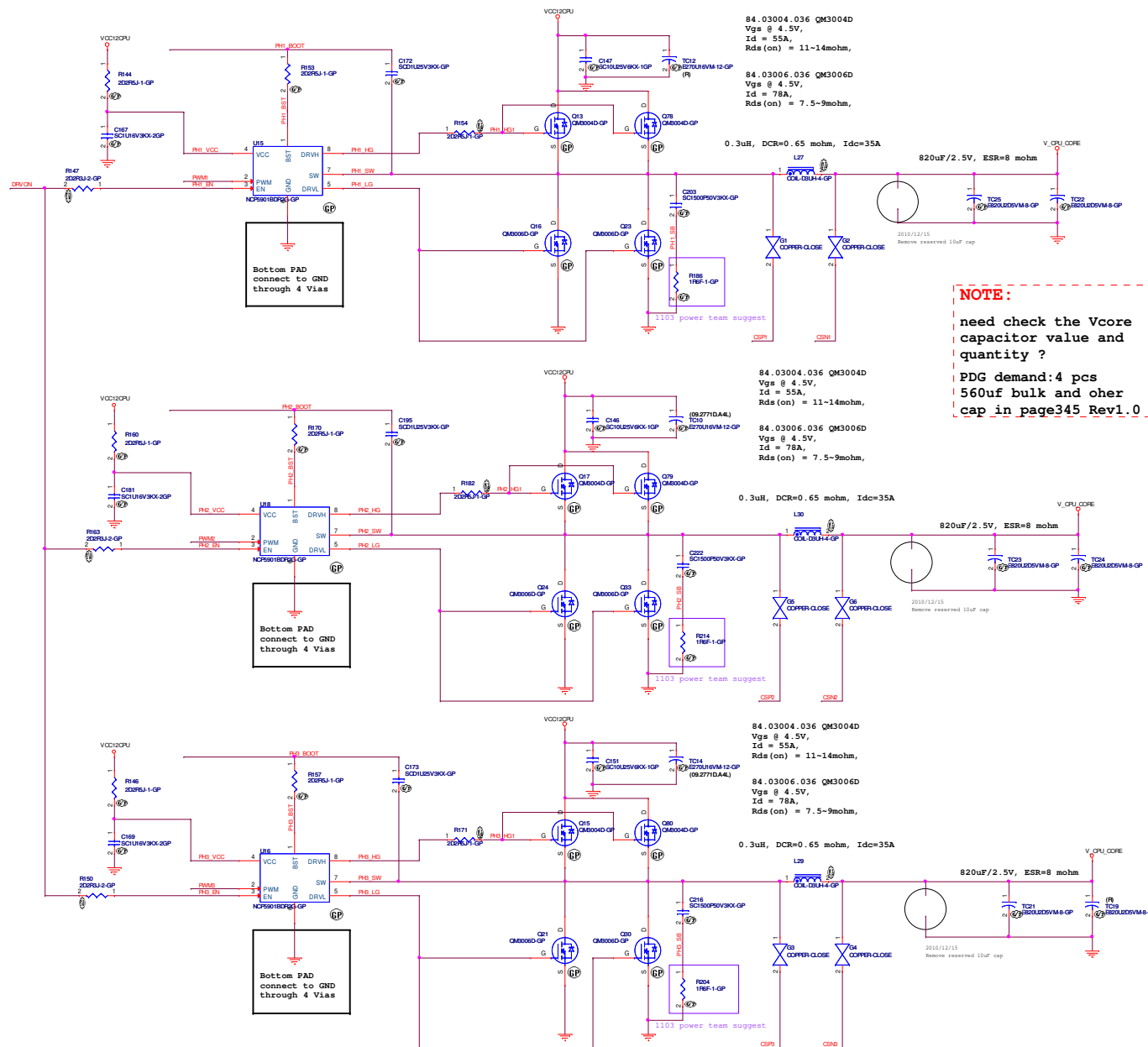
BOOT VOLTAGE	
Resistor value	Boot Voltage
10K	0V
25K	0.85V
45K	0.9V
70K	0.95V
95K	1V
124K	1.1V
155K	1.2V



CPU Vcore POWER

50 DRVON
50 PWM1
50 CSP1
50 CSN1
50 PWM2
50 CSP2
50 CSN2
50 PWM3
50 CSP3
50 CSN3

VCC_CORE



-Variant Name-

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Heilsh, Taipei
File	Document Number	Rev
Custom	P000_M000_H00_M00	SA
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